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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Production.

Revision 1.1: Update DEVICE ORDER INFORMATION.

Revision 1.2: Update V_{FB} Max limit to 0.82V in EC, add MSL.

I E E E G

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL
SCT2411TVBR	Tape & Reel	3000	2411	6	TSOT23-6L	1

F HG K H E G F

Over operating free-air temperature unless otherwise noted (1)

DESCRIPTION	MIN	MAX	UNIT
VIN, EN	-0.3	42	V
BST	-0.3	48	V
SW	-1		

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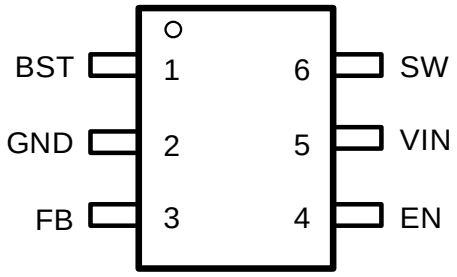

6-Lead Plastic TSOT23-6

E C E G G F

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	4.5	40	V
T_J	Operating junction temperature	-40	125	°C

F E G F

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001			

(6 '

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V_{IN}=12V, T_J=-40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		4.5		40	V
V_{IN_UVLO}	Input UVLO	V_{IN} rising		4.3		V
	Hysteresis			440		mV
I_{SD}	Shutdown current	EN=0, No load, VIN=12V		1	5	uA
I_Q	Quiescent current	EN=floating, No load, No switching. VIN=12V. BST-SW=5V		90		uA
Enable, Soft Start and Working Modes						
V_{EN_H}	Enable high threshold			1.21	1.4	V
V_{EN_L}	Enable low threshold		0.9	1.1		V
Power MOSFETs						
R_{DSON_H}	High side FET on-resistance			600		mΩ
R_{DSON_L}	Low side FET on-resistance			300		mΩ
Feedback and Error Amplifier						
V_{FB}	Feedback Voltage		0.78	0.8	0.82	V
Current Limit						
I_{LIM_HSD}	HSD peak current limit		1.2	1.5	1.75	A
I_{LIM_LSD}	LSD valley current limit	T_J=25°C	0.8	1	1.3	A
		T_J=-40°C~125°C	0.68			A
Switching Frequency						
F_{SW}	Switching frequency	V_{IN}=12V,				

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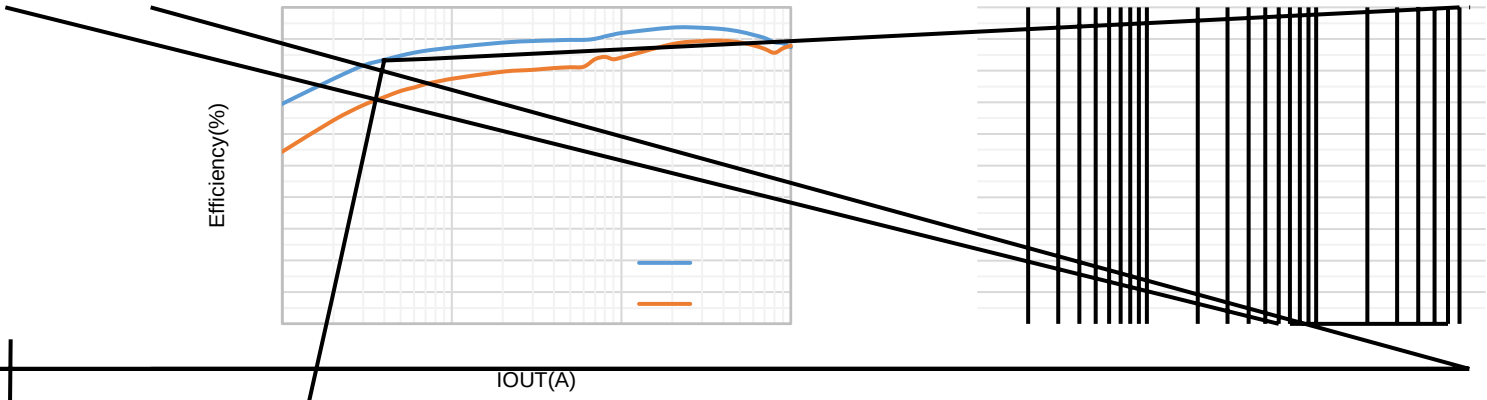

Figure 1. Efficiency vs Load Current, Vout=5V

Figure 2. Efficiency vs Load Current, Vout=12V

Figure 3. Load Regulation, Vout=5V, Vin=24V

Figure 4. Line Regulation, Vout=5V, Io=0.5A

Figure 5. Reference VS Temperature

Figure 6. HS Current Limit VS Temperature

GLC E G E FG F

Figure 7. LS Current Limit VS Temperature

Figure 8. Quiescent Current vs Temperature Vin=12V

H G E

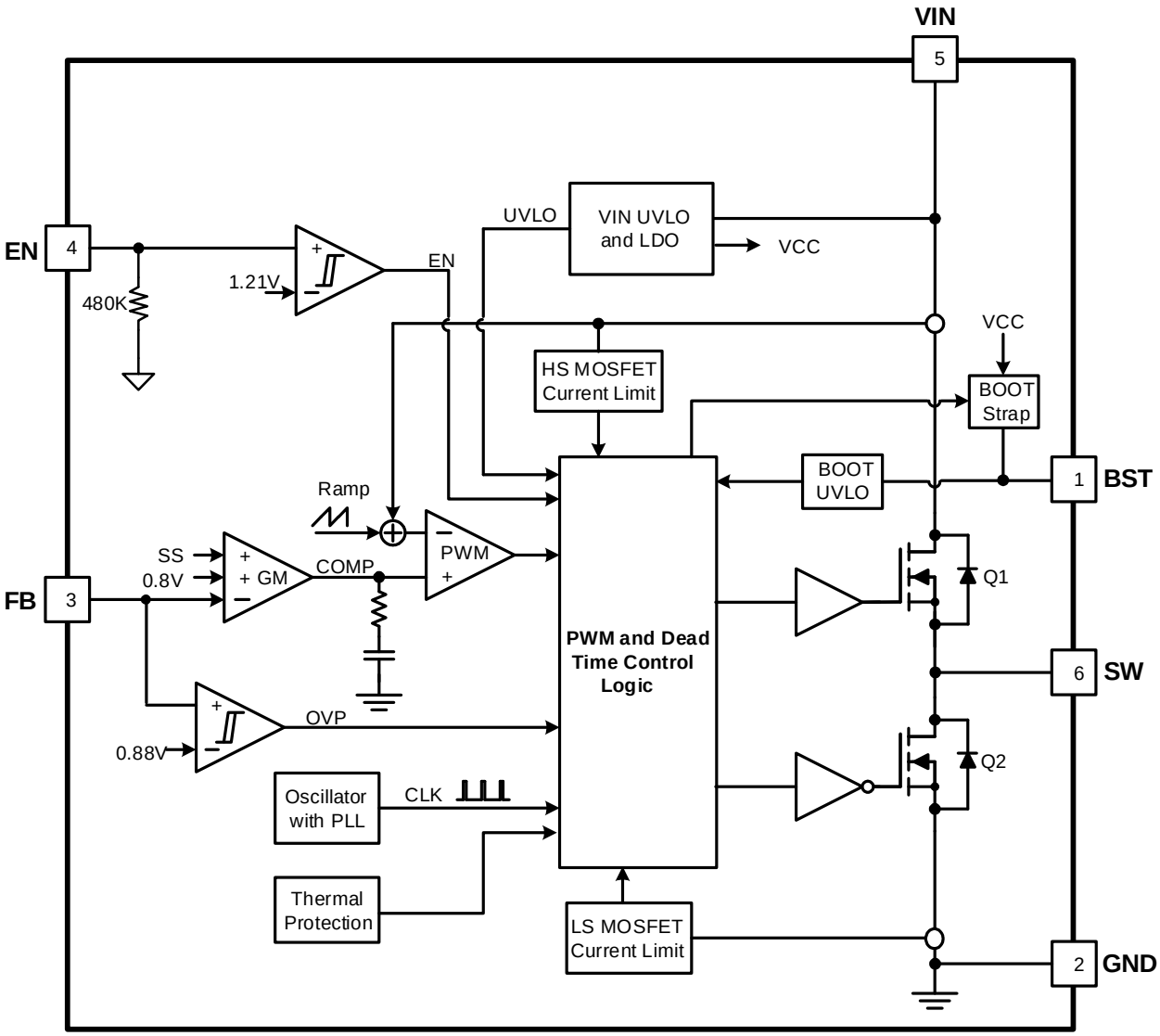

Figure 13. Functional Block Diagram

Overview

The SCT2411 device is 4.5V-40V input, 1A output, fully integrated synchronous buck converters. The device employs fixed frequency peak current mode control. An internal clock with 1.2MHz frequency initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly and the converter charges output cap. When sensed voltage on high-side MOSFET peak current rising above the voltage of internal COMP (see functional block diagram), the device turns off high-side MOSFET Q1 and turns on low-side MOSFET Q2. The inductor current decreases when MOSFET Q2 is ON. In the next rising edge of clock cycle, the low-side MOSFET Q2 turns off. This repeats on cycle-by-cycle based.

The peak current mode control with the internal loop compensation network and the built-in 1ms soft-start simplify the SCT2411 footprints and minimize the off-chip component counts. Meanwhile, it reduces the external passive components size as well.

The quiescent current of SCT2411 is 90uA typical under no-load and without switching condition. When disabling the device, the supply shut down current is only 1μA. The SCT2411 works at Pulse Skipping Mode PSM to further increase the power efficiency in light load condition.

Peak Current Mode Control and Pulse Skipping Mode

The SCT2411 employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the COMP voltage of the internal error amplifier, the high-side MOSFET turns off. The synchronous low-side MOSFET Q2 turns on till the next clock cycle begins or the inductor current falls to zero.

The error amplifier serves the COMP node by comparing the voltage of the FB pin with an internal 0.8V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage to the reference. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The SCT2411 operates in Pulse Skipping Mode (PSM) with light load current to improve efficiency. When the load current decreases, an increment in the feedback voltage leads COMP voltage drop. When COMP falls to a low clamp threshold (400mV typically), device enters PSM. The output voltage decays due to output capacitor discharging during skipping period. Once FB voltage drops lower than the reference voltage, and the COMP voltage rises above low clamp threshold. Then high-side power MOSFET turns on in next clock pulse. After several switching cycles with typical 160mA peak inductor current, COMP voltage drops and is clamped again and pulse skipping mode repeats if the output continues light loaded.

This control scheme helps achieving higher efficiency by skipping cycles to reduce switching power loss and gate drive charging loss.

VIN Power

The SCT2411 is designed to operate from an input voltage supply range between 4.5V to 40V, at least 0.1uF decoupling ceramic cap is recommended to bypass the supply noise. If the input supply locates more than a few inches from the converter, an additional electrolytic or tantalum bulk capacitor or with recommended 10uF may be required in addition to the local ceramic bypass capacitors.

Enable and Under Voltage Lockout UVLO

The SCT2411 Under Voltage Lock Out (UVLO) default startup threshold is typical 4.3V with VIN rising and shutdown threshold is 3.86V with VIN falling. The more accurate UVLO threshold can be programmed through the precision enable threshold of EN pin.

When applying a voltage higher than the EN high threshold (typical 1.21V/rising), the SCT2411 enables all functions

and the device starts soft-start phase. The SCT2411 has the built in 1ms soft-start time to prevent the output overshoot and inrush current. When EN pin is pulled low, the internal SS net will be discharged to ground. Buck operation is disabled when EN voltage falls below its lower threshold (typically 1.1V/falling).

An internal 480k pull down resistor make EN pin floating shut down the SCT2411

Peak Current Limit

The SCT2411 has cycle-by-cycle peak current limit with sensing the internal high side MOSFET Q1 current during overcurrent condition. While the Q1 turns on, its conduction current is monitored by the internal sensing circuitry. Once the high-side MOSFET Q1 current exceeds the limit, it turns off immediately. The maximum current passing through the power MOSFET is limited cycle-by-cycle. The switching frequency folds back to prevent an inductor current run-away during start-up or short circuit.

Bootstrap Voltage Regulator

An external bootstrap capacitor between BST and SW pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

The floating supply (BST to SW) UVLO threshold is 2.7V rising and hysteresis of 350mV. When the converter operates with high duty cycle or prolongs in sleep mode for certain long time, the required time interval to recharging bootstrap capacitor is too long to keep the voltage at bootstrap capacitor sufficient. When the voltage across bootstrap capacitor drops below 2.35V, BST UVLO occurs. The SCT2411 intervenes to turn on low side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee operation over a wide duty range.

Internal Soft-Start

The SCT2411 integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 0.8V reference voltage in 1ms. If the EN pin is pulled below 1.1V, switching stops and the internal soft-start resets.
The soft-start also resets during shutdown due to thermal overloading.

Over Current Protection

The SCT2411 implements over current protection with cycle-by-cycle limiting high-side MOSFET peak current and low-side MOSFET valley current to avoid inductor current running away during unexpected overload or output hard short condition. The inductor current IL is monitored during high-side MOSFET Q1 and low-side MOSFET Q2 on.

As shown in Figure 15, when overload or hard short happens, once the high-side MOSFET Ĭ ne m the-

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Over voltage Protection

The SCT2411 implements the Over-voltage Protection (OVP) circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load

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Typical Application

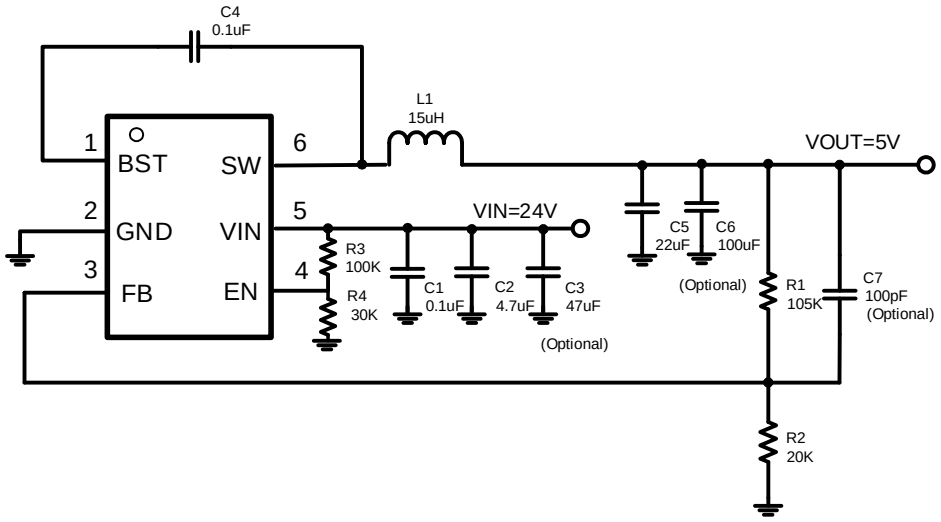

Figure 16. 24V Input, 5V/1A Output

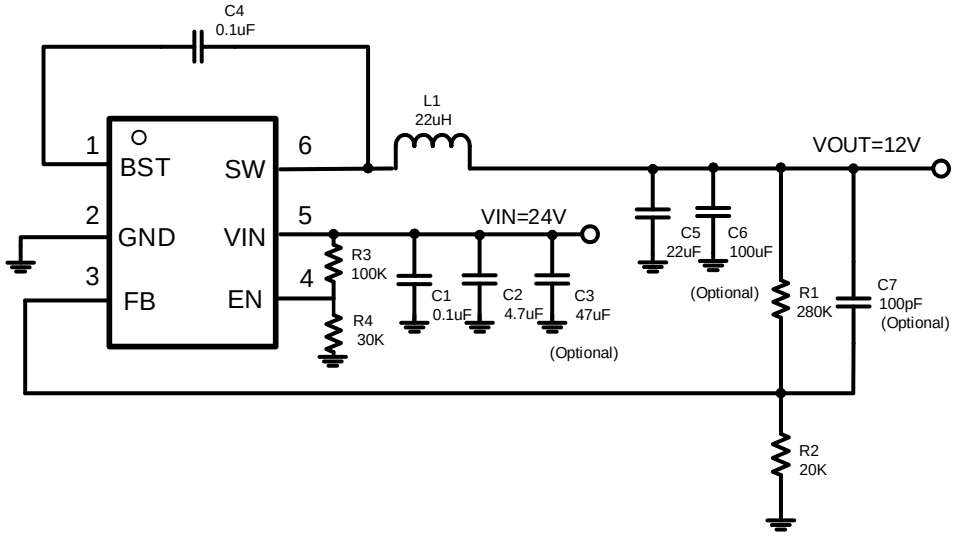

Figure 17. 24V Input, 12V/1A Output

Design Parameters

Design Parameters	Example Value
Input Voltage	24V
Output Current	1A
Switching Frequency	1.2MHz
Start Input Voltage (rising VIN)	5.5V
Stop Input Voltage (falling VIN)	5V

Output Voltage

The output voltage is set by an external resistor divider R1 and R2 in typical application schematic. Recommended R2 resistance is 20KΩ. Use Equation 4 to calculate R1.

(4)

where:

V_{REF} is the feedback reference voltage, typical 0.8V

d)) dn g ge e gf ml ml gd gge e lm !

V_{OUT}	R_1	R_2
1.8 V	24.9 KΩ	20 KΩ
2.5 V	42.2 KΩ	20 KΩ
3.3 V	62 KΩ	20 KΩ
5 V	105 KΩ	20 KΩ
12 V	280 KΩ	20 KΩ

Under Voltage Lock-Out

An external voltage divider network of R3 from the input to EN pin and R4 from EN pin to the ground can set the input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. For the

Where

L_{MIN} is the minimum inductance required
f_{sw} is the switching frequency
V_{OUT} is the output voltage
$V_{IN(max)}$ is the maximum input voltage
$I_{OUT(max)}$ is the maximum DC load current
LIR is coefficient of I_{LPP} to I_{OUT}

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in Equation 9 and Equation 10.

(9)

(10)

Where

I_{LPEAK} is the inductor peak current
I_{OUT} is the DC load current
I_{LPP} is the inductor peak-to-peak current
I_{LRMS} is the inductor RMS current

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 1.5A. The most conservative approach is to choose an inductor with a saturation current rating greater than 1.5A. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the SCT2411 can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a higher maximum output current.

15uH inductor value is recommended for

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increases.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 13 and the maximum input voltage ripple occurs at 50% duty cycle.

(13)

For this example, a 4.7μF, X7R ceramic capacitors rated of 50 V in parallel are used. And a 0.1 μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 14 desired.

(14)

Where

Δ is the output voltage ripple
f_{SW} is the switching frequency
L is the inductance of inductor
C_{OUT} is the output capacitance
V_{OUT} is the output voltage
V_{IN} is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, one 22μF ceramic output capacitors work for most applications.

Application Waveforms

V_{IN}=24V, V_{OUT}=5V, unless otherwise noted

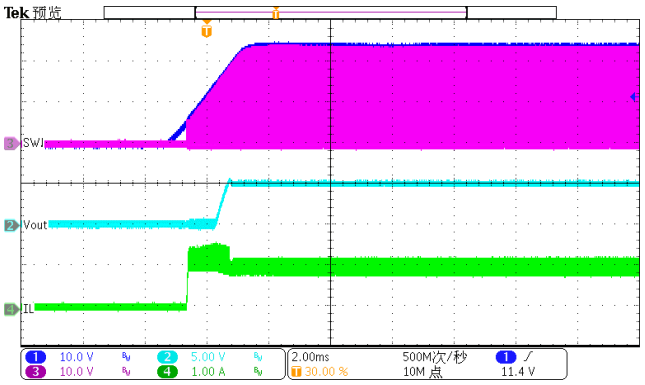

Figure 18. Power up (I_{LOAD}=1A)

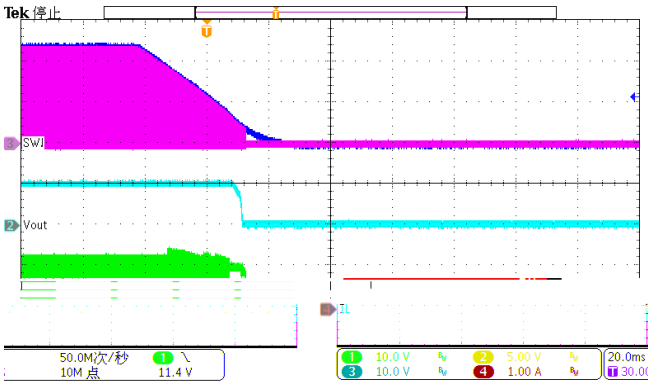

Figure 19. Power down (I_{LOAD}=1A)

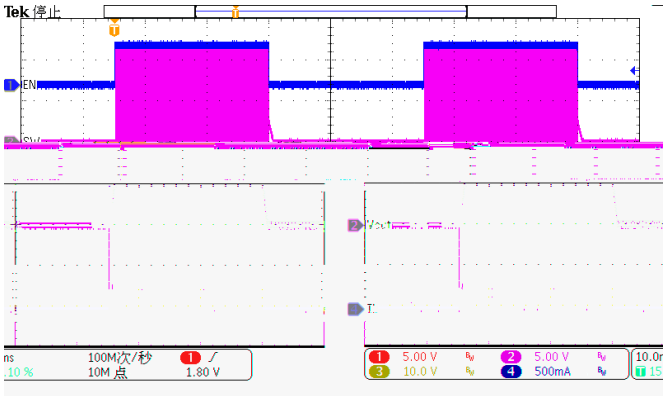

Figure 20. EN toggle (I_{LOAD}=0.01A)

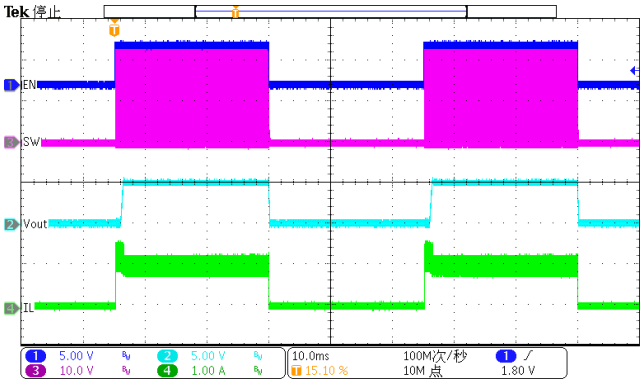

Figure 21. EN toggle (I_{LOAD}=1A)

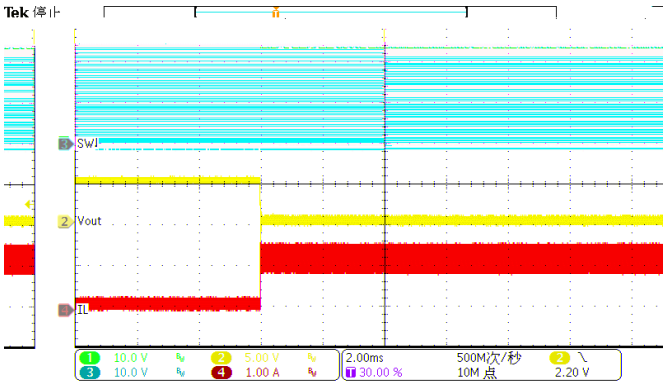

Figure 22. Over Current Protection (0.1A to hard short)

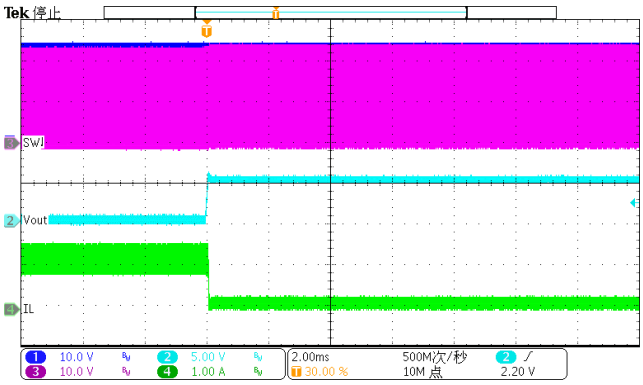

Figure 23. Over Current Release (hard short to 0.1A)

Application Waveforms

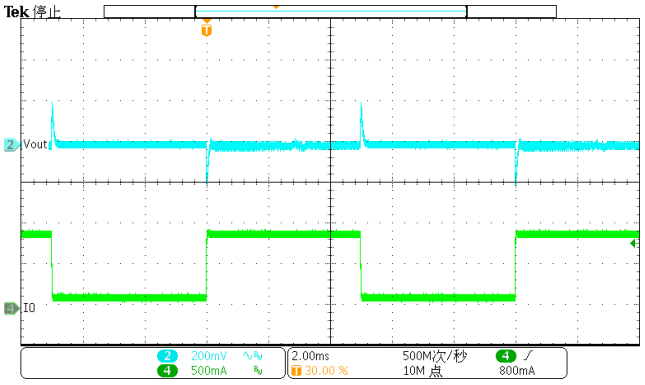

Figure 24. Load Transient (0.1A-0.9A, 1.6A/us)

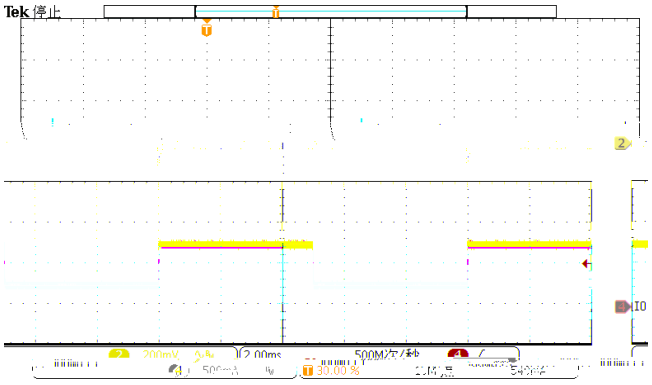

Figure 25. Load Transient (0.25A-0.75A, 1.6A/us)

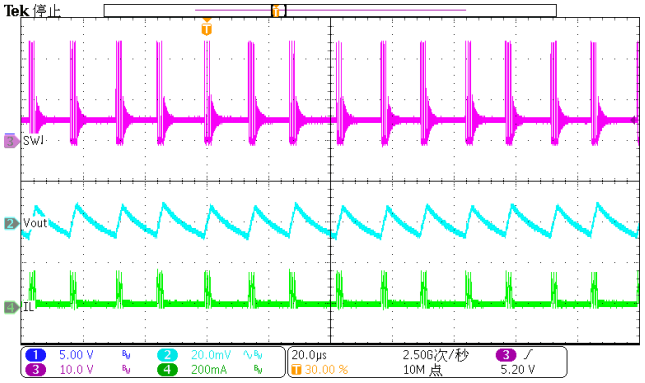

Figure 26. Output Ripple (I_{LOAD}=10mA)

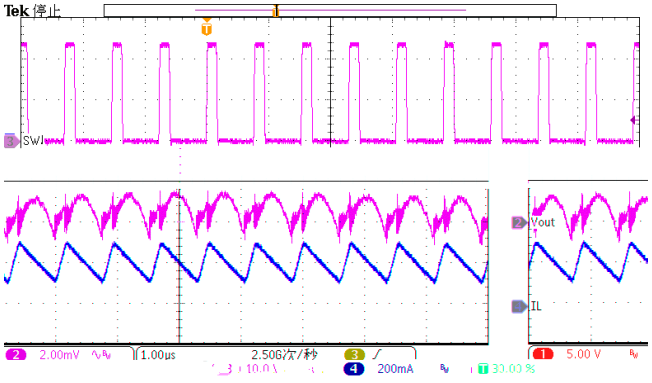

Figure 27. Output Ripple (I_{LOAD}=0.2A)

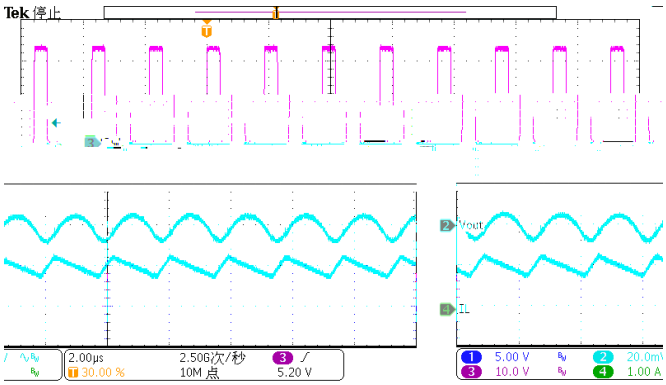

Figure 28. Output Ripple (I_{LOAD}=1A)

Figure 29. Thermal, 24V_{IN}, 5V_{OUT}, 0.8A

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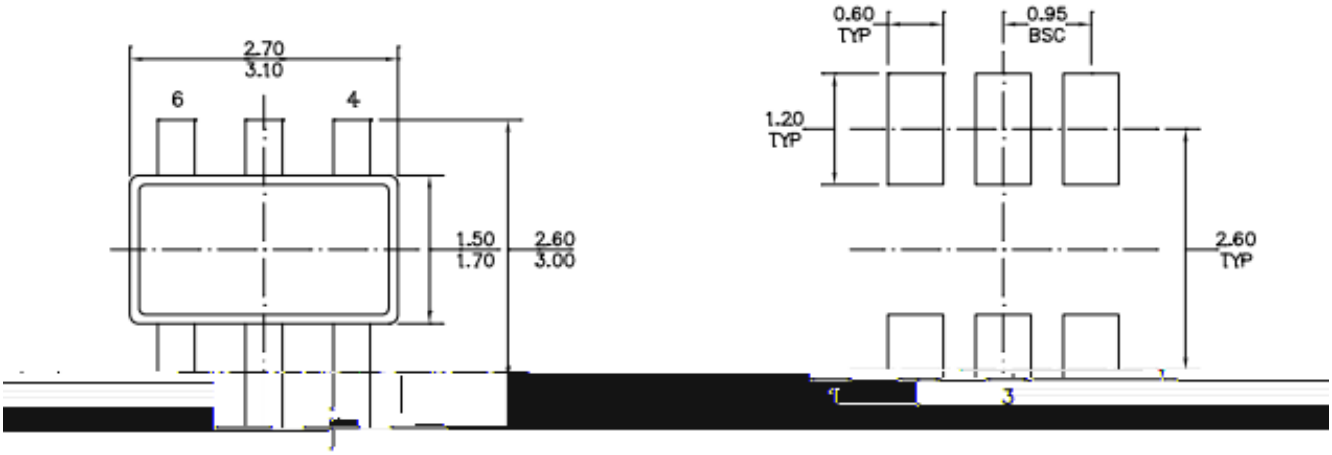
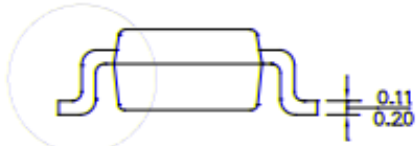
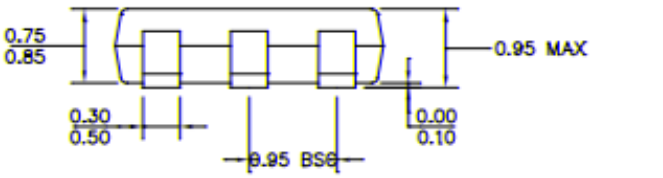


RECOMMENDED LAND PATTERN **TOP VIEW**





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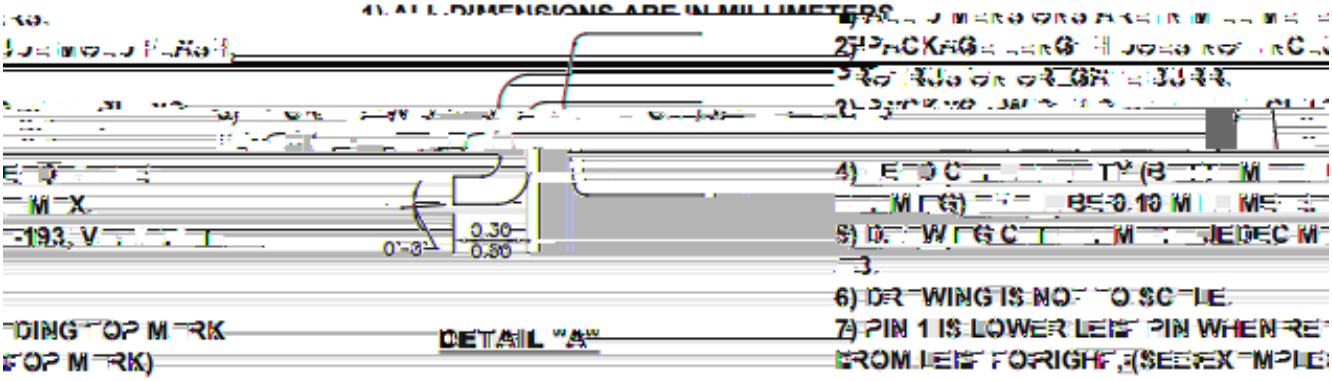

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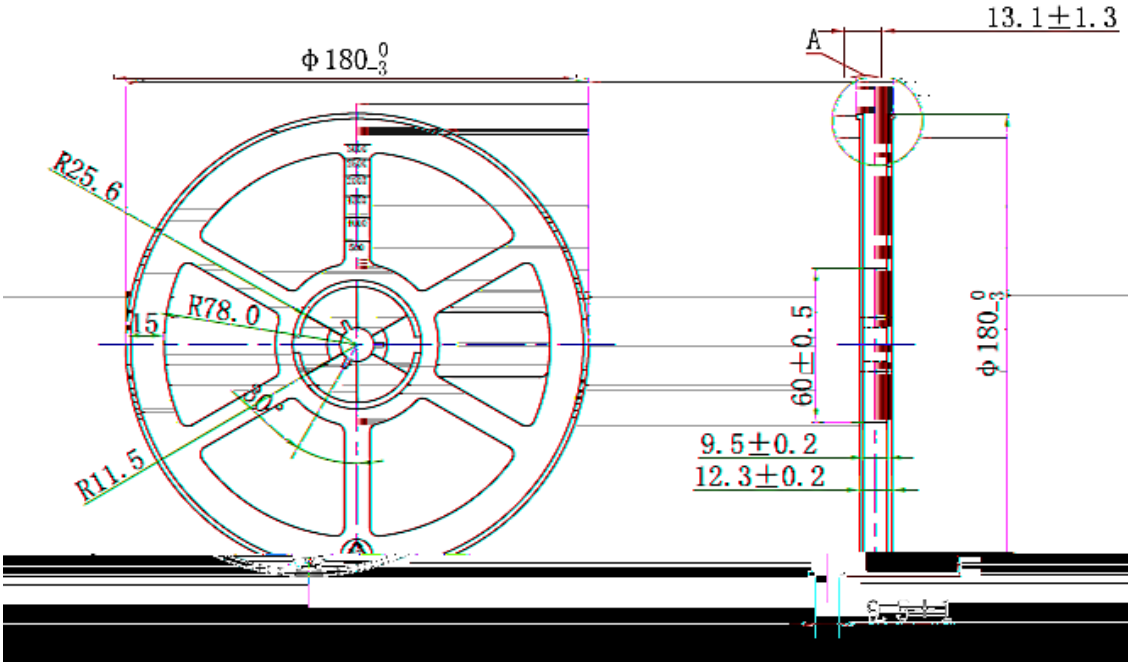

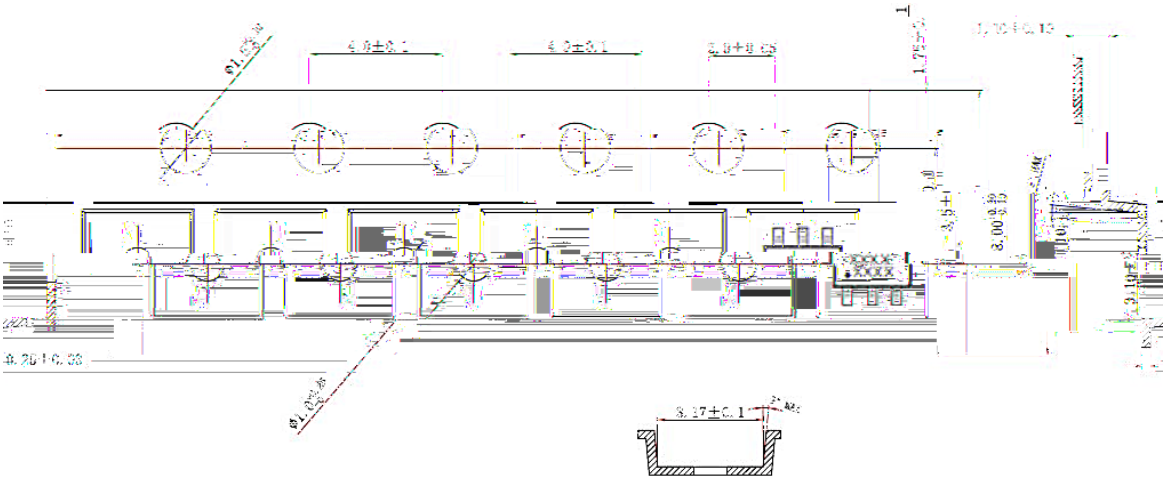

Feeding Direction

