

SCT71801A00 Series

REVISION HISTORY

(). ; A H G< L I LJL C L CCH G; >C L U G J; A H G< L B = LL H L CH
, CCH , F; I JU > =CH

DEVICE ORDER INFORMATION

Orderable Device	Output Voltage	Package	Package Marking	PINS	MSL	Transport Media, Quantity
- . . ,	>D	-) &				.; J , F

PIN CONFIGURATION



RECOMMENDED OPERATING CONDITIONS

) L I J L ; G G J L L L HA H F I B L C H >

PARAMETER	DEFINITION	MIN	MAX	UNIT
0 (	HJ I F; A L HA			0
0) /.	) J I F; A L HA			0
0 (	H <F GJ I F; A		0 (	0
0	I LAI > JG I F; A			0
& 3	U AL; GG; <F I L II > F . G			0
(	HJ =; J; =Q L			
) /.	) J =; J; =Q L			
-,	) J =; J; =Q L -, L K G H			
.	) J L ; GADH CH GJ L L			

ABSOLUTE MAXIMUM RATINGS

) L I J L ; G G J L L L HA H F I B L C H >

PARAMETER	DEFINITION	MIN	MAX	UNIT
0 (	; G G GJ I F; A L HA			0
0) /.	; G G I J I F; A L HA			0
0	; G G ><; =EJG I F; A			0
0 (	; G G H <F GJ I F; A		0 (	0
0	; G G JI LAI > JG I F; A			0
0 &	; G G JI LAI >> F JG I F; A			0
.	H CH GJ L L L HA			
. A	- I L A GJ L L L HA			

- (1) - L < I H B F > H L < I F ; G G ; GAG; = ; > G J LG; H H >; G; A . B > G CH A; L H > I
H CH I G I C, =GG H >) J L CH I H CH
- (2) = U H GCL CIL B F < =H = >< H ; H B J F > JJI L A 0) / . I L I B L JI L J J F 1 B H B J F >
JJI L C B B L B; H 0 B G; G G U H & G C C < L F L B; H I J U = B 4 H L
- (3)) J L ; CH G B C L HA ; I G J LG; H H > G >; G; A B A B F = L G; F J L I LG; H CH A; L H > I G B I J L ; G A
; G < CH GJ L L L HA

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
0 .	G; H I > I > F J L (- - J =G; CH ; FJG			E0
	B; LA > G I > F J L (- - J =G; CH ; FJG			E0

- (1) >I = G H ; B; 0 ; H ; G; H ; = L G A G; ; H; L > - = H U F J U =
- (2) >I = G H ; B; 0 ; H ; G; H ; = L G A G; ; H; L > - = H U F J U =

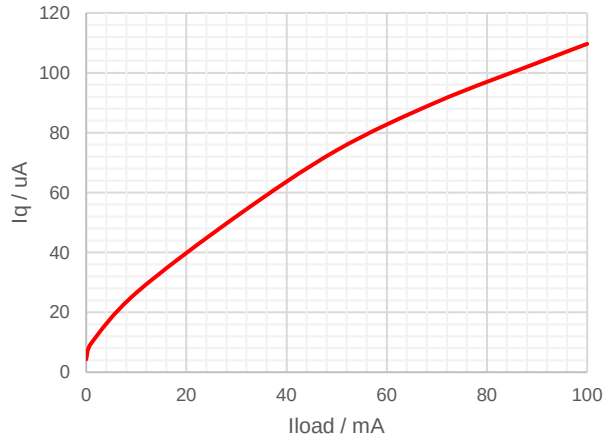
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ELECTRICAL CHARACTERISTICS

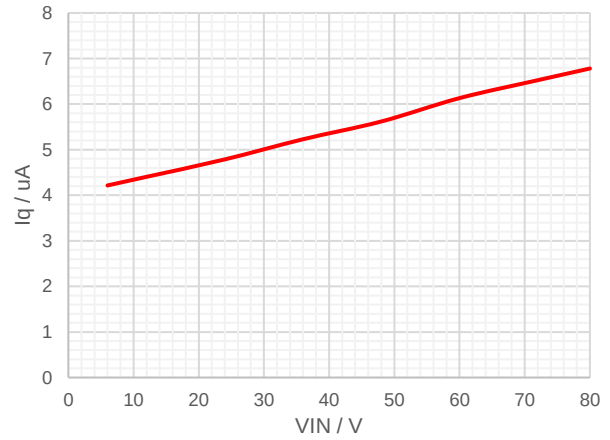
0 (0) / . 0) / . . JG; F; F C > H L

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
0 (	) J L; @A@U I F; A					0
0 / 0 &)	0 (/ 0 &) . BL BI F L C	0 (LC@A				0 G0
- (	- B > I H = LL H LL G 0 (J@	(0 (0 (0 (0				
+	+ C = H = LL H LL G (J@	(F; H F; > 0 (0 .				
		(F; H F; > 0 (0 .				
		(F; H F; > 0 (0 .				
		(F; H F; > 0 (0 .				
		(F; H F; > 0 (0 .				
Regulated Output Voltage and Current						
0	><; =E I F; A ; = L; =	. .				0 0
0) / .	&@ L A F @H	0 (0) / . 0 I 0				G0
	&; > L A F @H	I G I G				G0
0 ,)	LL JI I F; A	0 (0) / . 0 I G				G0
		0 (0) / . 0 I G				G0
) / .	) J = LL H	0) / . @L A F @H				G
)	) J = LL H @G C					G
)	) L LL H I F; <; =E	0 (0 (9 0				G
- , ,	I L JJF LD = @H L; @	0) / . 0 I G E) / .				>
		0) / . 0 I G E) / .				>
		0) / . 0 I G E) / .				>
		0) / . 0 I G E) / .				>
Enable and Soft-startup						
0 (9	H < F B@B BL BI F					0
0 (9 &	H < F F BL BI F					0
0 (9	H < F BL BI F B L C					G0
(9 0	H < F J@J F J = LL H	(0				
. . .	- I ; L @					G
Power Good						
0 9,	LC@A BL BI F J L = H; A	0) / . 0) / . () B H 0) / . LC@A				
0 9	; @A BL BI F J L = H; A	0) / . 0) / . () B H 0) / . ; @A				
0 3-	LQ B L C					
0 9 & 1	I J F I F; A	VOUT=0.8XVOUT(NOM), PG sink 100uA		76		G0

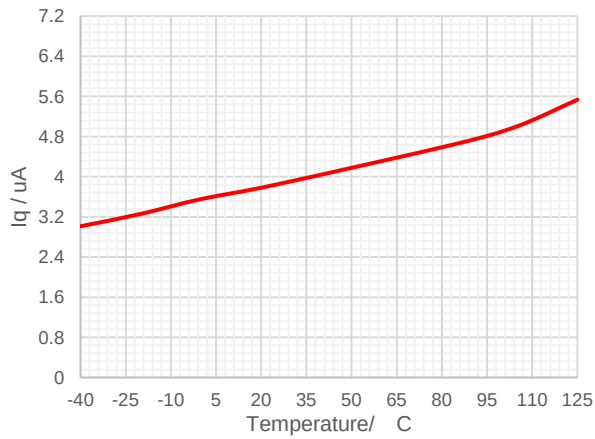
TYPICAL CHARACTERISTICS



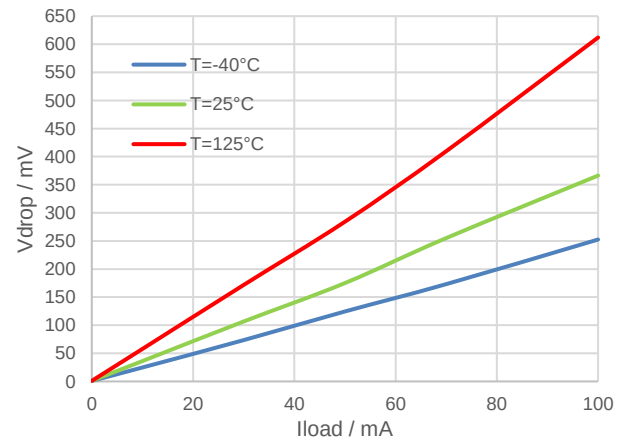
① L + C = H LL H) J LL H



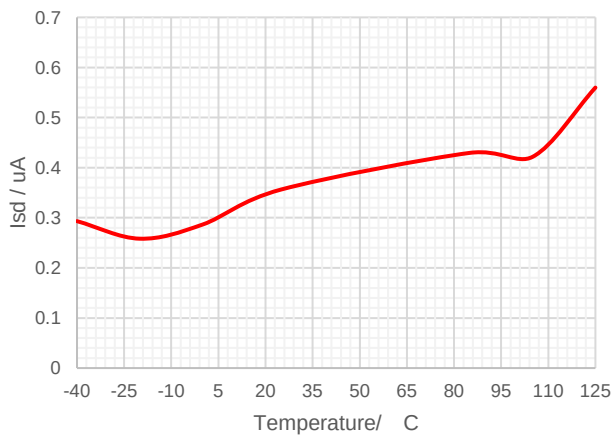
① L + C = H LL H HJ 01 F; A (1 F; >



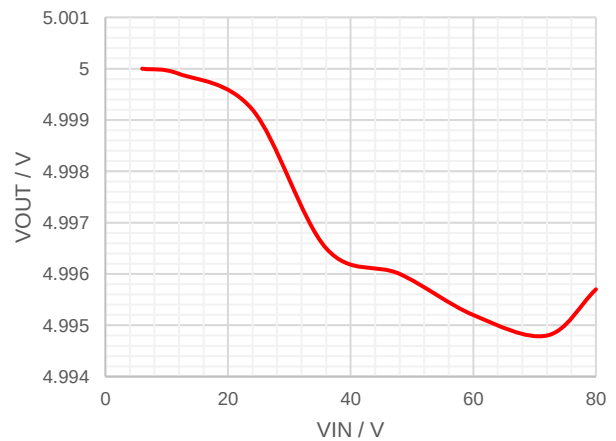
① L + C = H LL H G<CH. GJ L; L



① L LL JI 01 F; A) J LL H

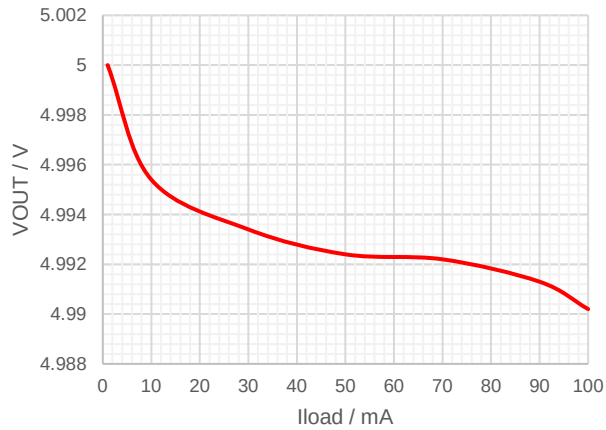


① L -B >1 H LL H G<CH. GJ L; L

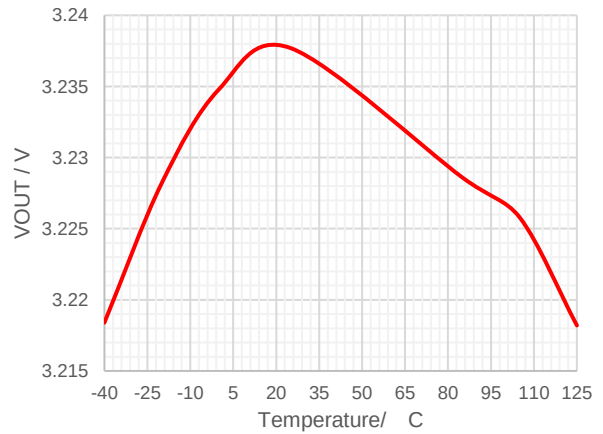


① L) J 01 F; A HJ 01 F; A

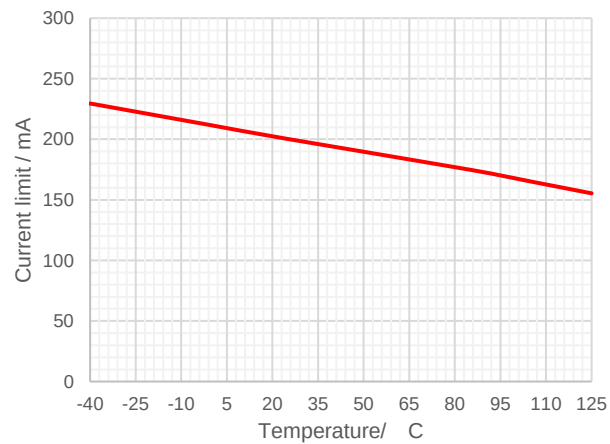
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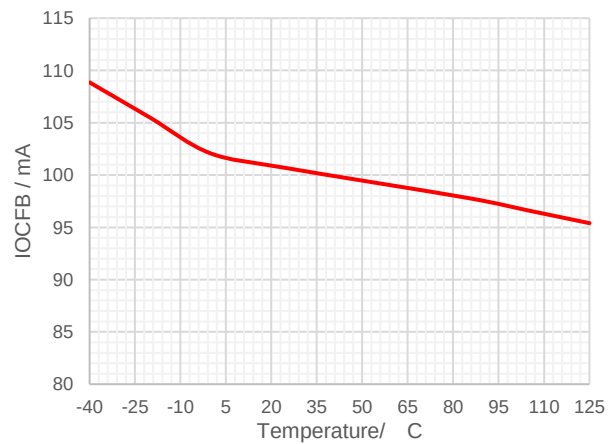
AL) J 0IF;A) J LL H



AL) J 0IF;A G<CH. GJ L; L ;
0) / . 0



AL) J LL H & CC G<CH. GJ L; L ;
0 (0



AL) J LL H & CC G<CH. GJ L; L ;
0 (0

TYPICAL CHARACTERISTICS (continued)



0) / . Ø L - , , L K H=) / . G

0 (Ø L - , , L K H= J) / . G

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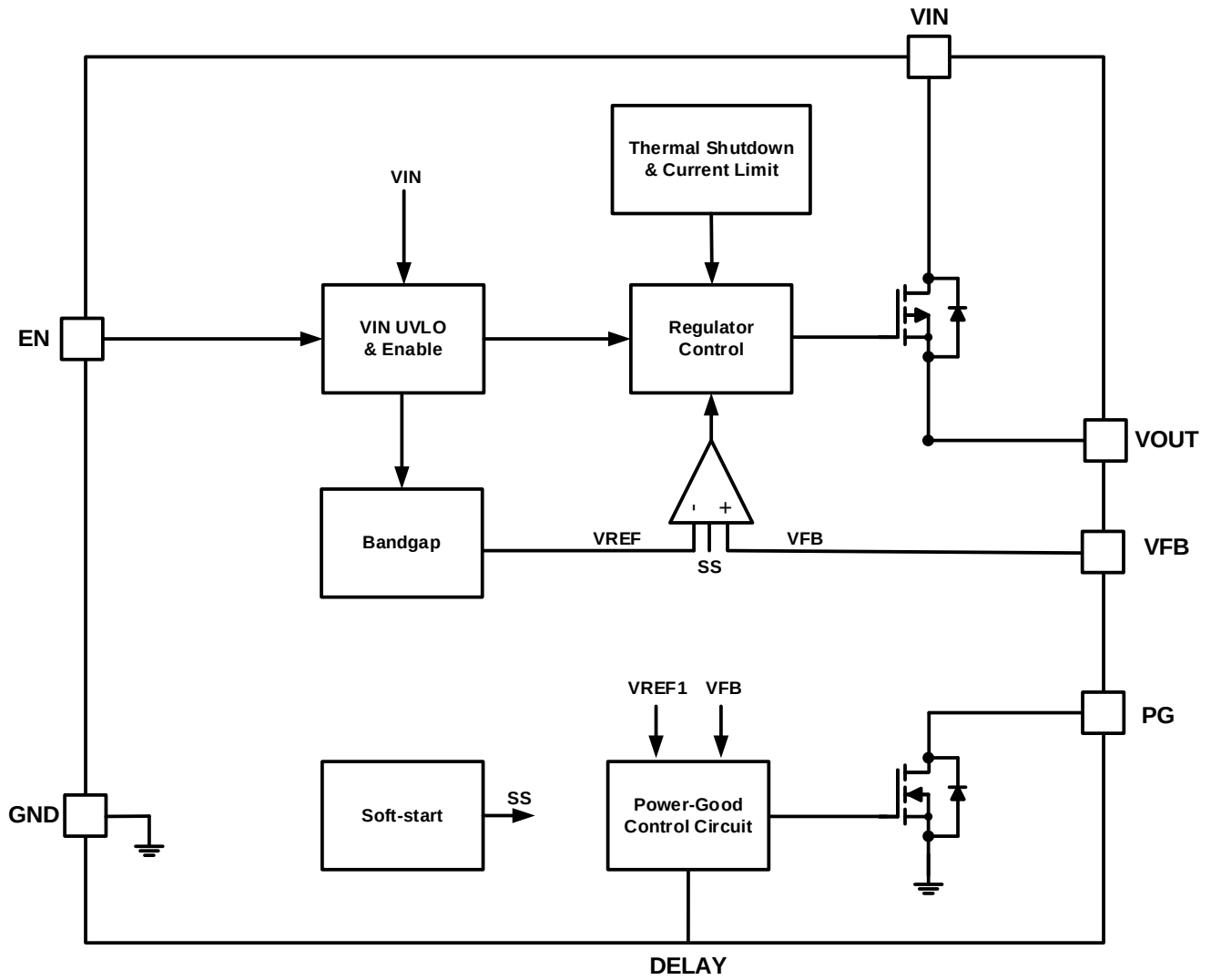
TYPICAL CHARACTERISTICS (continued)



0 (0 0 L - , , L K H J) / .) / . G

0 (0 0 L - , , L K H J) / . J) / .

FUNCTIONAL BLOCK DIAGRAM



Q L H C H F F = E C A L G I > D) J O L C H

OPERATION

Overview

. B - . LC JII > = ; L G 0 0 I F; A L; HA 0; LL A F; IL 0 B L F K C = H
= LL H . B I F; A L A F; IL I J L; U G 0 I 0 0 I F; A ; H = H G K C = H = LL H;
H F; >
. B - . LC JII > = C ; < F 0 I J = J; = 0 L ; H = L; G 0 = J; = 0 L C
L = G G H > H 0 I H F I ; L 0 ; I 0 F; LA 0 L B = LL H ; H I J I F; A I L B I > L 0 A
; L J
. B - . LC JII > = ; F I JII 0 H < F = H U F I L I I > ; L ; H JII A; G G; < F I L
I I > > F 0 B 0 B C L G < F I L B ; J J 0; CH H > 0 A K H = H 0 L; CH) B L JII = CH
; L 0 F > B 0 (0 H H L I F; A F = B I L = LL H JII = CH I J B; L > B L JII = CH; H
B L G; F B > H JII = CH
. B - . LC JII > = JII 0 ; > D ; < F I J L CH U G 0 I 0 I H > ; H I J
I F; A L CH I L; H J; = E A I J CH J F; FL I = H; = - . ; F

Enable and Under Voltage Lockout Threshold

. B - . LC JII > = C H < F > B H B 0 (J 0 I F; A L C ; < I 0 ; H B (J 0 I F; A
= > B H < F B L B I 0 (9 . B > 0 C > C; < F > B H B 0 (J 0 I F; A ; F < F 0 I L B H B
(J 0 I F; A C < F 0 (9 & H U F J F J = LL H I L = I (J 0; H B > 0 H < F B H (J 0 F;
I L; B 0 B L G / 0 &) B L B I 0 = H H ; H U F L C I L > C 0 L , ; H , U G 0 (I (B I H 0
0 L . B / 0 &) L C 0 A; H ; 0 A B L B I 0 = H < = F F > < K ; CH ; H K ; CH L J = C F

1 B L

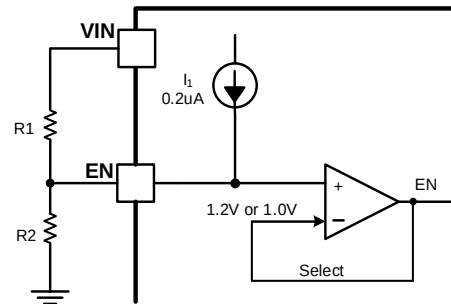
0 (LC 0 0 I L C B L B I 0 I H < F B > 0

0 (B 0 0 I B L C B L B I 0

; H = 0 < H A F = > 0 B = F F CH

0 (9 0

0 (9 & 0



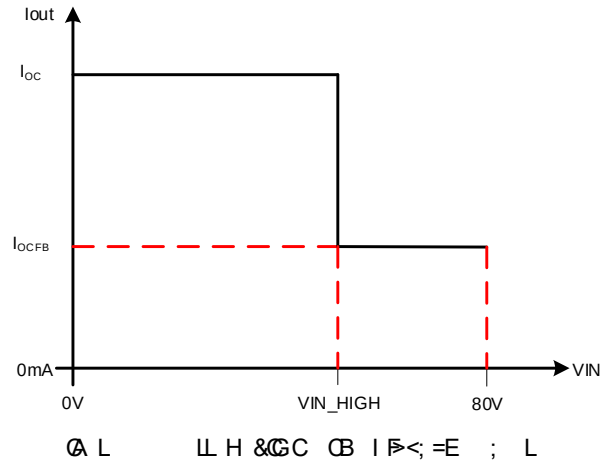
0 L - G / 0 &) < H < F > C 0

Regulated Output Voltage

1 B H B 0 I F; A C B 0 B L B; H 0) / . () 0 ,) I J J 0 C B L A F > I J < ; > I H B L K C >
I F; A L CH 1 B H B 0 I F; A ; F < F 0) / . () 0 ,) I J J 0 L; = E B 0 I F; A G 0 B
> U J I F; A < ; > I H B F; > = LL H 1 B H B 0 I F; A > U J < F / 0 &) B L B I 0 B I J E J
B I 0 &) H I B

. B I J I F; A C H L A F; > B H B > @ C @ = L H R C 1 B H; = L H R C H I = L B
L A F; I L < A C I B; J < =; I B C L; @ J I L > C Q; C H B L G; F B > I H C L A L > B > @
I H I L B > @ = I F > I H B @ I H; F B L G; F B > I H = C C I H B > @ < = E I H B I J
= L H; F = H > C H J L C B > @ = F < H = L H R C; H > B L G; F B > I H

1 C B B I L = L H VIN_HIGH Control ; L B - . LC J I I > = I F < G I L I I < ; H
; L B H I L = L H; F; H > B I L C A H I = L C; F I L K C B G; C G F; > C A = L H B I F
< G; F L B; H) > L C A; L J . B = B; L = L C @ C B I H C B I F C A @ L

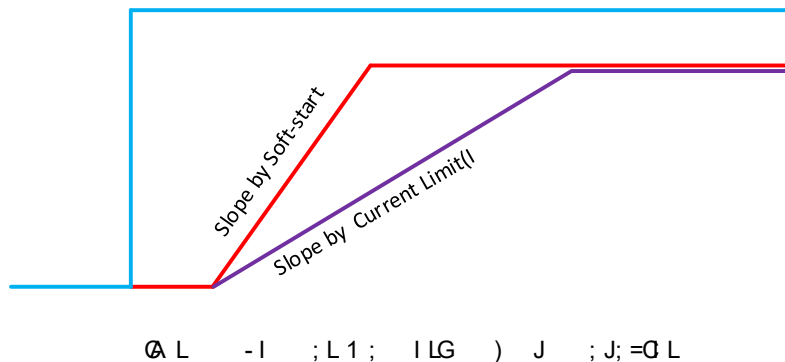


Internal Soft-Start

. B - . LC J I I > = @ A L; ; H @ I H F I ; L = C C B; L G J B L L H I F; A I I G
I I F I 0 L L H I F; A @ B (J C J I F > < I F 0 &) C < B I ; H > B @ I H F
I ; L L . B I ; L; F I L > L C A B > I H > I B L G; F I I F; > C A

I F @ L B I B ; L J ; I L G; G; F I J = J; = Q L; H > F I A I J = J; = Q L 1 B H I J
= J; = Q L C G; F I L ; G J F B I F J I 0) / . C R C < I ; L 1 B H I J = J; = Q L C F I A I L
; G J F B I F J I 0) / . C R C > < = L H R C) ; 0 (VIN_HIGH ; H > B I F J I 0) / . C
R C > < = L H R C) B H 0 (VIN_HIGH

H - . LC J I I > = J @; F. C ; H > J @; F) C G ; H > J @; F) C G = F
B I F C A I L G F I L C C F ; L J C = F F C H



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Power-Good and Power-Good Delay

When the power-good delay is enabled, the PG output is high-impedance when V_{OUT} exceeds V_{IT} , and V_{DELAY} exceeds V_{REF} . The power-good delay time can be calculated using: $t_{DELAY} = (C_{DELAY} \times V_{REF}) / I_{DELAY}$. For example, when $C_{DELAY} = 10 \text{ nF}$, the PG delay time is approximately 12 ms; that is, $(10 \text{ nF} \times 1.2\text{V}) / 1 \mu\text{A} = 12 \text{ ms}$.

When C_{DELAY} is used, the PG output is high-impedance when V_{OUT} exceeds V_{IT} , and V_{DELAY} exceeds V_{REF} . The power-good delay time can be calculated using: $t_{DELAY} = (C_{DELAY} \times V_{REF}) / I_{DELAY}$. For example, when $C_{DELAY} = 10 \text{ nF}$, the PG delay time is approximately 12 ms; that is, $(10 \text{ nF} \times 1.2\text{V}) / 1 \mu\text{A} = 12 \text{ ms}$.

When the power-good delay is enabled, the PG output is high-impedance when V_{OUT} exceeds V_{IT} , and V_{DELAY} exceeds V_{REF} . The power-good delay time can be calculated using: $t_{DELAY} = (C_{DELAY} \times V_{REF}) / I_{DELAY}$. For example, when $C_{DELAY} = 10 \text{ nF}$, the PG delay time is approximately 12 ms; that is, $(10 \text{ nF} \times 1.2\text{V}) / 1 \mu\text{A} = 12 \text{ ms}$.

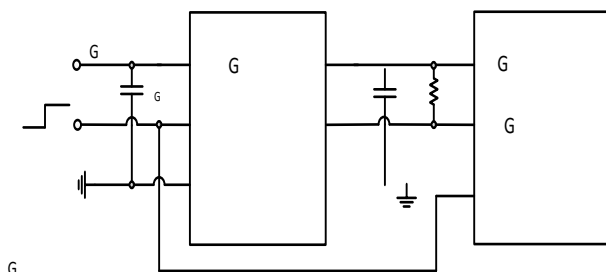


Figure 1. Power-Good Delay Circuit

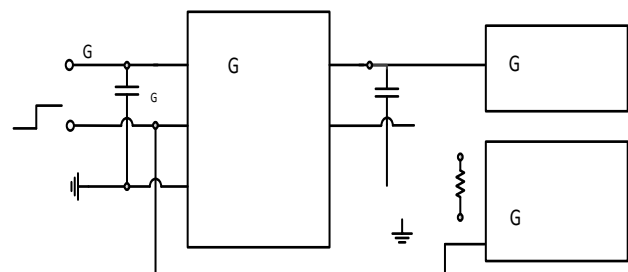
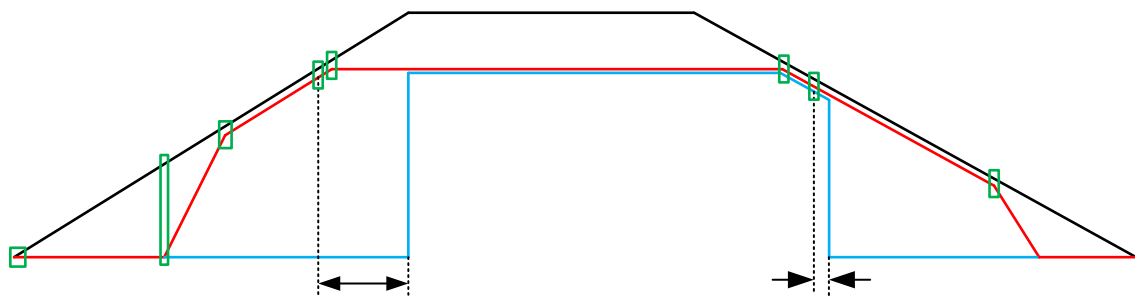


Figure 2. Power-Good Delay Circuit

When the power-good delay is enabled, the PG output is high-impedance when V_{OUT} exceeds V_{IT} , and V_{DELAY} exceeds V_{REF} . The power-good delay time can be calculated using: $t_{DELAY} = (C_{DELAY} \times V_{REF}) / I_{DELAY}$. For example, when $C_{DELAY} = 10 \text{ nF}$, the PG delay time is approximately 12 ms; that is, $(10 \text{ nF} \times 1.2\text{V}) / 1 \mu\text{A} = 12 \text{ ms}$.



④ L - ; L J ; H - B > I H ; GJF - . - LC

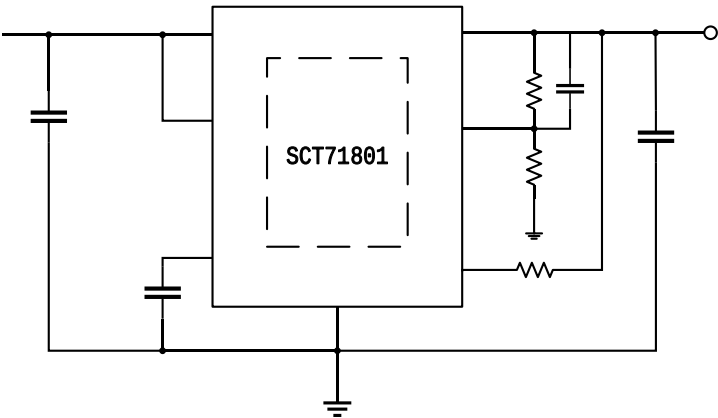
Thermal Shutdown

. BC> ⑥ CH WJ L ; B LG; F B > I H . - = C C ; ; J L = CH U G I LB ; ④ A I L = H G I H LG; F I J L ; CH B D H CH GJ L ; L B I H = > B . . L Q J I ④ . B D H CH GJ L ; L = > ④ A B . -

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APPLICATION INFORMATION

Typical application 1:

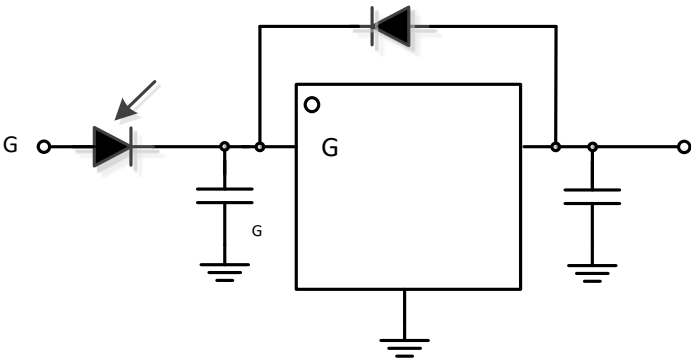


Q L - . . JG; F JJG; CH- =B G; G

Design Parameters

Design Parameters	Example Value
HJ 0I F; A	0 (I LG; F 0 0
) J 0I F; A	0 I L 0 0
; G G) J LL H	G
) J ; J; =Q L, ; HA	L = GG H>
HJ ; J; =Q L, ; HA	L = GG H>
FF J L C I L I JI LAI> ,	E

Typical application 2:



Q L - . . JG; F JJG; CH- =B G; G CB, L I F; LC C>

Design Parameters	
Design Parameters	Example Value
HJ 0I F; A	0 (I LG; F 0 0
) J 0I F; A	0 I L 0 0
; G G) J L H	G

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Output Voltage

. B I J I F; A C < ; H I H FL C I L > C O L, ; H, C I J E; F; J J E; C H = B G; E, = I G G H >
, L C; H C E / K; C H I =, F F,

B L

0, C B >< = E L L H I F; A J E; F 0

Table 1: Compensation Values for Typical Output Voltage/Capacitor Combinations

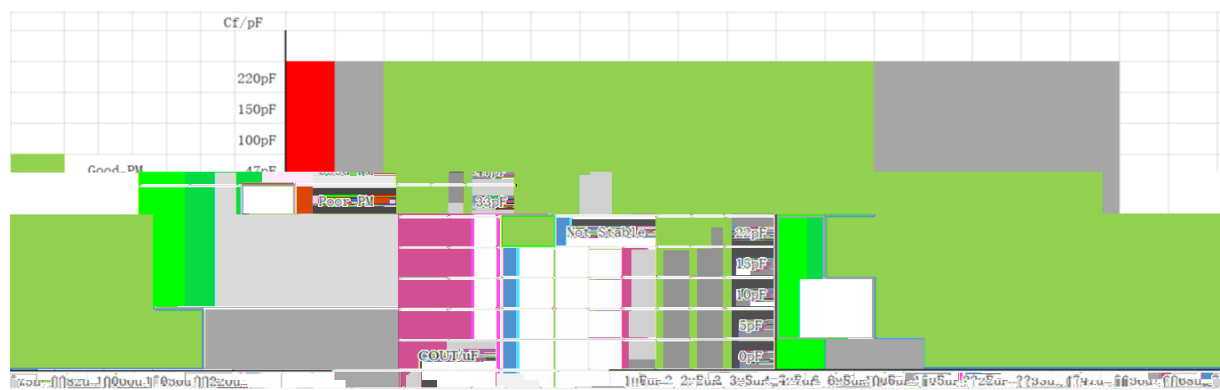
0I 0	) /.	J	, E	, E	) /. I J C H F - ,

Input Capacitor and Output Capacitor

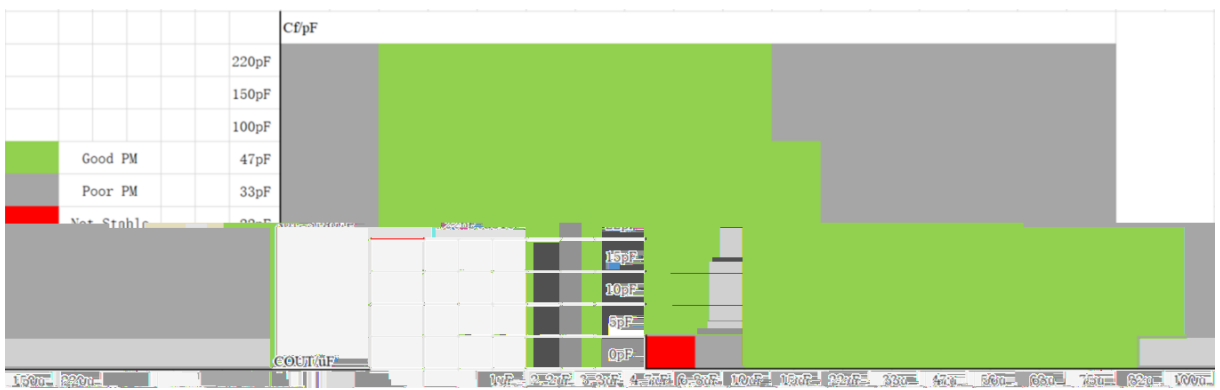
- . L = I G G H > ; >> C A; I L A L; L = J; = Q L C B; < J; = J; = Q L C H J; L; F F; 0 (J C I E J
B C U I F; A ; < F F G C G F = U F E = J; = Q L I L I B L = J; = Q L C B B O B = J; = C H C A A > I L
B G J I L C B F L A I F; A J E . B I F; A L; C A I B = J; = Q L G < A L; L B; H B G; C G
C U I F; A

. I H L F I J ; < C B - . J U > = L K C ; H I J = J; = Q L C B; G C C G = C
= J; = C H ; F I H > B J U > = = F J J I L I J = J; = Q L L; H A U G I ; H > C B
; H -, L; H A < H ; H - . L = I G G H > F = C A; 2 , I L 2 , J = L; G E
= J; = Q L C B F -, I L G J L; L L; H A I C J U B F; > L; H C H L J I H

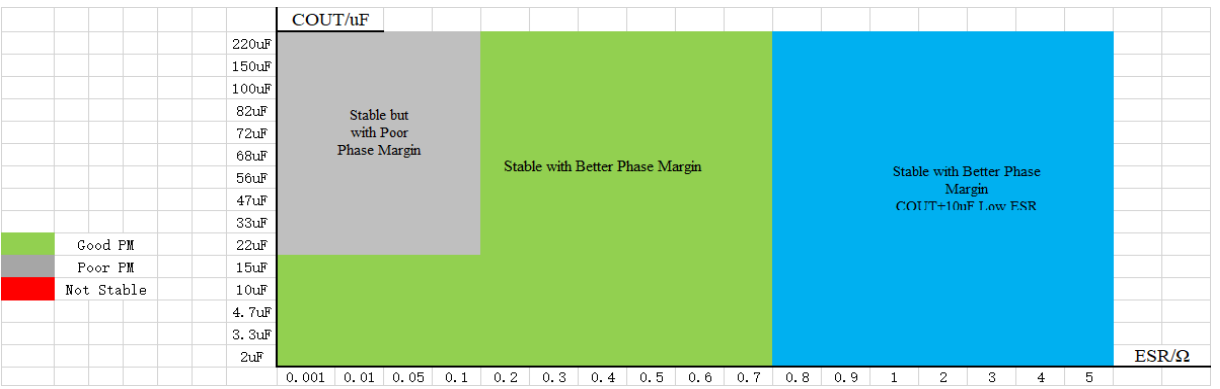
1 B H C A F L A I J = J; = Q L C B B O B L -, L C I L I L ; G J F I J F = U F E = J; = Q L C B
-, L C I L C B ; J J E; C H - . L = I G G H > ; >> C A L; F -, I J = J; = Q L J; L; F F
= H H = C H C B B F L A F = U F E = J; = Q L B C C F C C B H L B I I L B I I F; A = > < B
F L A -, L C I L; H A < L F; > L; H C H J L I L G; H



ω_L - . $> 1/L; L > J; = Q L L \neq G G \Rightarrow$, $E(0)/.$ 0



ω_L - . $> 1/L; L > J; = Q L L \neq G G \Rightarrow$, $E(0)/.$ 0



ω_L - . - ; $< Q(0 -) J$; $J; = Q L$

SCT71801A00 Series

Power Dissipation and Thermal Performance

$P_{D(TH)} = P_{D(TH)} \times \left(\frac{T_{J(TH)} - T_{J(TH)}}{T_{J(TH)} - T_{J(TH)}} \right)$
 $P_{D(TH)} = P_{D(TH)} \times \left(\frac{T_{J(TH)} - T_{J(TH)}}{T_{J(TH)} - T_{J(TH)}} \right)$

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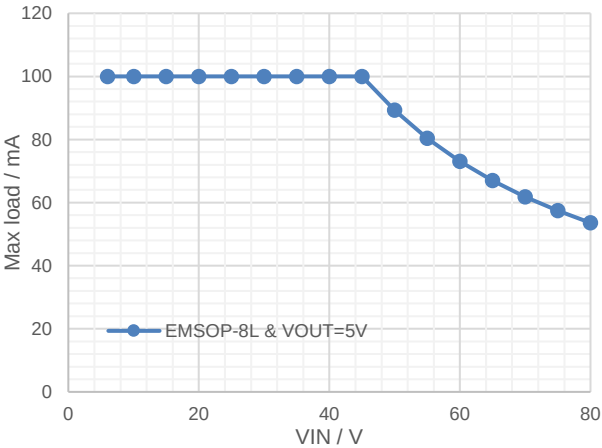
$P_{D(TH)} = P_{D(TH)} \times \left(\frac{T_{J(TH)} - T_{J(TH)}}{T_{J(TH)} - T_{J(TH)}} \right)$
 $P_{D(TH)} = P_{D(TH)} \times \left(\frac{T_{J(TH)} - T_{J(TH)}}{T_{J(TH)} - T_{J(TH)}} \right)$

$P_{D(TH)} = P_{D(TH)} \times \left(\frac{T_{J(TH)} - T_{J(TH)}}{T_{J(TH)} - T_{J(TH)}} \right)$

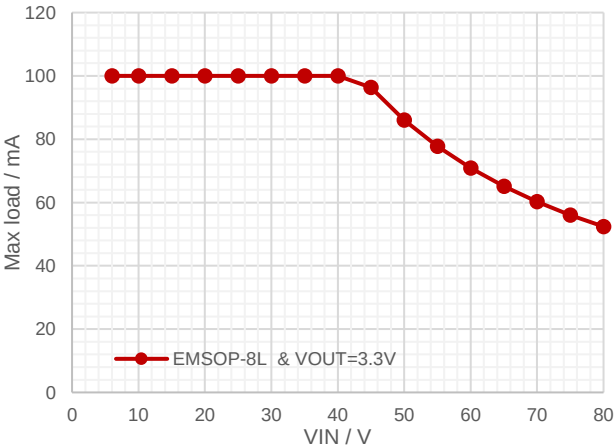
Thermal Performance of Different Packages Based on EVM Test

Package	Max Allowable PD (W) (Not Trigger TSD,VOUT=5V)	Max Allowable PD (W) (TJ≤150)	R JA_EVM (°C/W)
-) &			

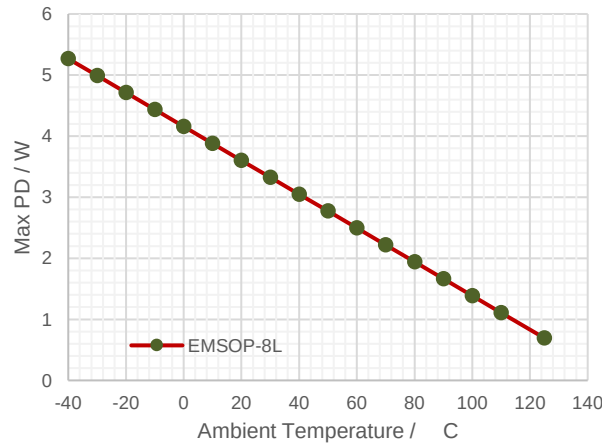
THERMAL CHARACTERISTICS



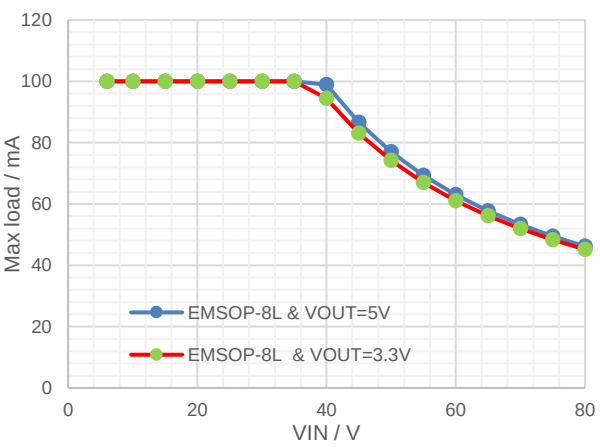
④ L ; ④ G) J LL H HU 0IF; A
0) / . 0I >C L H J; =E A . . - 9,



④ L ; ④ G) J LL H HU 0IF; A
0) / . 0I -) & . . - 9,



④ L ; ④ G ④ > I L C Q; ④ H G<CH
. GJ L; L -) &.

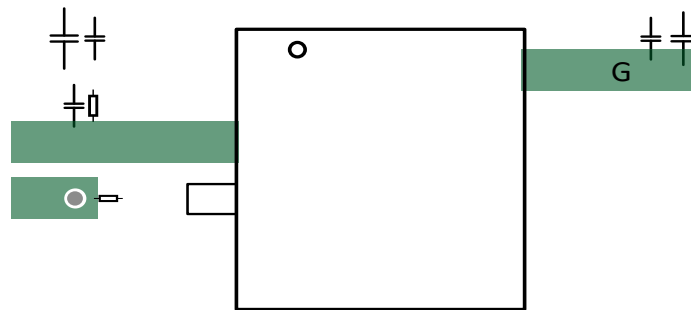


④ L ; ④ G) J LL H HU 0IF; A
-) &.

SCT71801A00 Series

Layout Guideline

1. I BCU = J; = Q L ; H I J = J; = Q L G < J F = > ; = F I B > @ J C I ; J I G F
2. C L = G G H > I < J; B C U J C I A I H > C B ; < J; = J; = Q L . B F I J ; L ; I L G > < B < J; = J; = Q L = H H = C H 0 (J C I ; H B (J C I B G G < ; G ; F ; J I G F
3. C L = G G H > I @ L ; = F H A B I L B G E = J J L @ B I G C C C , > I J ; H B ; > C Q ; C H
4. . I C J U B B L G ; F J L I L G ; H I B > @ ; H G ; C C B = I L H I J ; B @ B ; G < C H G J L ; L - . L = G G H > J L ; > C A B = J J L H > L B B L G ; F J ; > ; L ; J I G F ; H J F = C A H A B B L G ; F C I H B = J J L H > L B B L G ; F J ; >
5. C A F I A F = I F @ = J; = Q L C B @ B - , L C I L - . L = G G H > ; > > C A ; F - , = J; = Q L J ; L ; F F = H H = C H C B B F I A F = I F @ = J; = Q L



Q L & I ; G J F

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