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PIN FUNCTIONS

NAME	PIN	PIN FUNCTION
PGND3	1	**Power ground for Buck3.** Should be electrically connected to the system power ground plane with the shortest and lowest-impedance connection possible.
SW3	2	**Buck3 switch node.** SW is the output of the internal power switch. Connect to an external inductor using a wide PCB trace.
VIN23	3	**Input supply voltage for Buck2 and Buck3.** VIN23 assumes to connect to the output of Buck1. Place a ceramic decoupling capacitor (10uF) from VIN23 to PGND2/3.
SW2	4	**Buck2 switch node.** SW is the output of the internal power switch. Connect to an external inductor using a wide PCB trace.
PGND2	5	**Power ground for Buck2.** Should be electrically connected to the system power ground plane with the shortest and lowest-impedance connection possible.
VOUT2	6	**Feedback for Buck2.** Connect VOUT2 pin to the Buck2 output directly.
GPIO1	7	**General Purpose Input/Output pin1.** GPIO1 can be configured as INTB or VMON.
VCC	8	**Internal VCC regulator output.** Power supply to the internal control circuit and gate drivers. A 1uF decoupling capacitor to ground close to this pin is required.
AGND	9	**Analog ground.** AGND is the reference GND for the internal logic and signal circuit. AGND is not internally connected to Power Ground, make sure AGND connected to power ground in PCB.
LDOOUT	10	**LDO4 output.** Connect a 4.7uF or higher ceramic capacitor between this pin and ground.
VOUT1	11	**Feedback for Buck1 and power source for LDO4.** Connect VOUT1 pin to Buck1 output directly. A decoupling capacitor to ground is recommended to be placed close to VOUT1 pin to minimize switching spikes.
PGND1	12	**Power ground for Buck1.** Should be electrically connected to the system power ground plane with the shortest and lowest-impedance connection possible.
SW1	13	**Buck1 switch node.** SW is the output of the internal power switch. Connect to an external inductor using a wide PCB trace.
VIN	14	**Input supply for the device and Buck1.** A decoupling capacitor to ground is recommended to be placed close to VIN pin to minimize switching spikes.
BST	15	**Bootstrap capacitor connection pin for Buck1.** Connect a 0.1uF ceramic capacitor between this pin and SW1.
GPIO2	16	**General Purpose Input/Output pin2.** GPIO2 can be configured as SEQOUT, PG, GPO, INTB, ERRIN, WDI, SLEEPB or RSTIN.
RESETB	17	**Reset Output.** High state of this pin indicates all channels work properly and low state indicates power rails are not ready or a fault condition. RESETB could be configured as either open-drain or push-pull. Float this pin if not used.
SCL	18	**Serial clock line.** Connect this pin to ground if not used.
SDA	19	**Serial data line.** Open-Drain I/O, connect this pin to a high level via a pull-up resistor. Connect this pin to ground if not used.
VOUT3	20	**Feedback for Buck3.** Connect VOUT3 pin to the Buck3 output directly.

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SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{LDO4_DROP}	Dropout voltage	V_{OUT1}=3.3V, V_{LDO4} set to 3.3V, I_{LDO4}=300mA		120	240	mV
L_{LINE_REG4}	Line Regulation	V_{OUT1}=3V to 5V, V_{LDO4} set to 2.7V, I_{LDO4}=100mA		0.02		%/V
L_{LOAD_REG4}	Load Regulation	V_{OUT1}=3.3V, V_{LDO4} set to 2.8V, I_{LDO4}=10mA to 300mA		0.1		%
I_{LIM_OCP4}	Over-current limit	V_{OUT1}=3.3V, V_{LDO4} set to 2.8V	320	400	500	mA
I_{LIM_SCP4}	Short-circuit current limit	V_{OUT1}=3.3V, V_{LDO4}=0V	40	70	100	mA
PSRR(1)	Power supply rejection ratio	V_{OUT1}=3.3V, V_{LDO4}=2.8V, C_{LDO4}=4.7uF, I_{LDO4}=100mA, @ 10kHz		60		dB
		V_{OUT1}=3.3V, V_{LDO4}=2.8V, C_{LDO4}=4.7uF, I_{LDO4}=100mA, @ 100kHz		60		dB
		V_{OUT1}=3.3V, V_{LDO4}=2.8V, C_{LDO4}=4.7uF, I_{LDO4}=100mA, @ 1MHz		40		dB
N_{RMS}(1)	RMS Noise	V_{OUT1}=3.3V, V_{LDO4}=2.8V, C_{LDO4}=4.7uF, I_{LDO4}=100mA, from 10Hz to 100kHz		30		μV_{RMS}
R_{DIS4}	Output discharge resistance	Output disabled		50	100	Ω
Protection						
V_{OV_R}	Output over-voltage rising threshold		106	108	110	%
V_{OV_HYS}	Output over-voltage hysteresis			2		%
V_{UV_F}	Output under-voltage falling threshold		90	92	94	%
V_{UV_HYS}	Output under-voltage hysteresis			2		%
V_{DPOV_R}	Output deep over-voltage protection rising threshold	DEEP_OVP_SEL[1:0]=00		115		%
		DEEP_OVP_SEL[1:0]=01		112		%
		DEEP_OVP_SEL[1:0]=10		110		%
		DEEP_OVP_SEL[1:0]=11		108		%
V_{DPOV_HYS}	Output deep over-voltage protection hysteresis			2		%
V_{DPUV_F}	Output deep under-voltage protection falling threshold	DEEP_UVP_SEL[1:0]=00		75		%
		DEEP_UVP_SEL[1:0]=01		80		%
		DEEP_UVP_SEL[1:0]=10		85		%
		DEEP_UVP_SEL[1:0]=11		90		%
V_{DPUV_HYS}	Output deep under-voltage protection hysteresis			2		%
t_{HICCUP}	Hiccup time		72	80	88	ms
T_{WR}	Thermal warning rising threshold		140	155	170	°C
T_{WR_HYS}	Thermal warning hysteresis			20		°C
T_{SD}	Thermal shutdown rising threshold		160	175	190	°C
T_{SD_HYS}	Thermal shutdown hysteresis			20		°C
RESETB						
$V_{OL\_RSTB\_OD}$	Open-drain output low level voltage	I_{SINK}=1mA			0.1	V

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SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$I_{LKG\_RSTB\_OD}$	Open-drain output high leakage current		-1		1	uA
$V_{OL\_RSTB\_PP}$	Push-pull output low level voltage	I_{SINK}=1mA			0.1	V
$V_{OH\_RSTB\_PP}$	Push-pull output high level voltage	$V_{IO[0]}$=0	3	3.3	3.6	V

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SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
t_{LOW}	Low period of the SCL clock		500			ns
t_{HIGH}	High period of the SCL clock		260			ns
t_{HD_STA}	Hold time (repeated) START condition		260			ns
t_{SU_STA}	Set-up time for a repeated START condition		260			ns
t_{HD_DAT}	Data hold time		0			ns
t_{SU_DAT}	Data set-up time		50			ns
t_{SU_STO}	Set-up time for STOP condition		260			ns
t_r	Rise time of both SCL and SDA signals				120	ns
t_f	Fall time of both SCL and SDA signals				120	ns
C_B	Capacitive load for each bus line				550	pF

(1) Guaranteed by sample characterization, not tested in production.

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TYPICAL CHARACTERISTICS

V_{IN} = 10V, V_{OUT1} = 3.3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{OUT4} = 2.8V, L1 = 2.2uH, L2 = L3 = 1uH, FCCM, T_A = 25°C, unless otherwise noted.

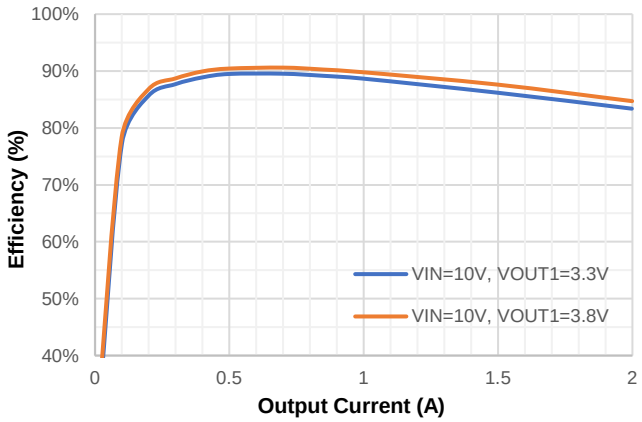

Figure 1. Buck1 Efficiency vs. Load Current

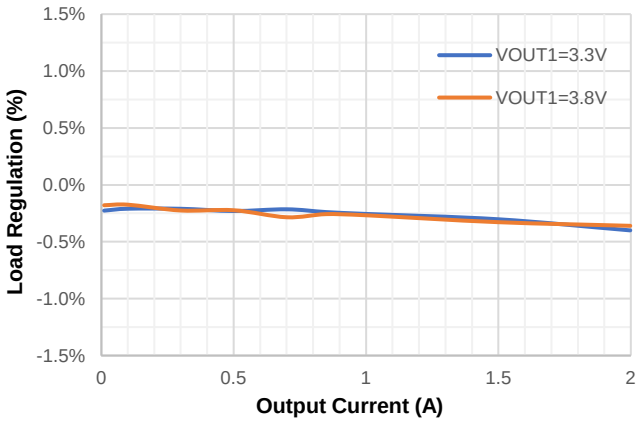

Figure 2. Buck1 Load Regulation

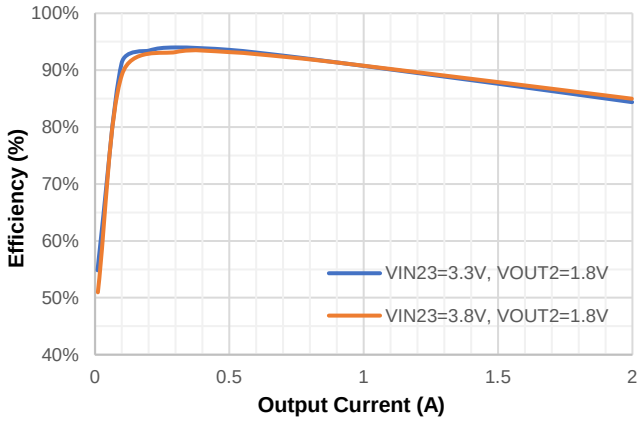

Figure 3. Buck2 Efficiency vs. Load Current

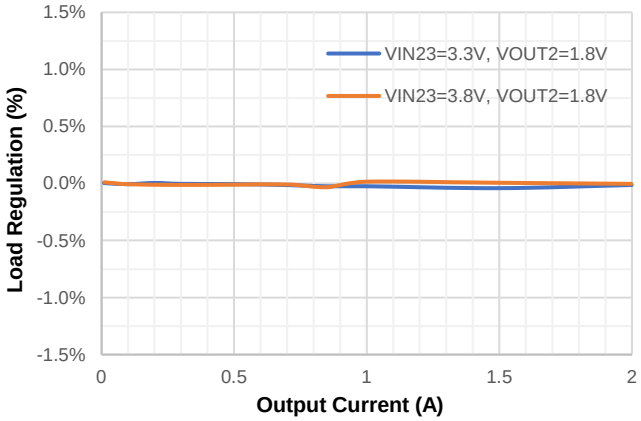

Figure 4. Buck2 Load Regulation

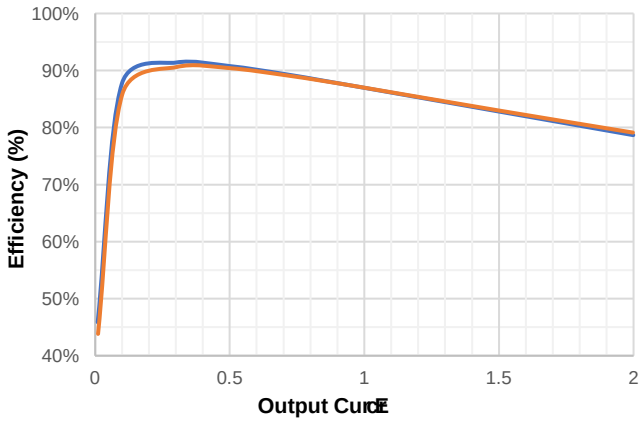

Figure 5. Buck3 Efficiency vs. Load Current

Figure 6. Buck3 Load Regulation

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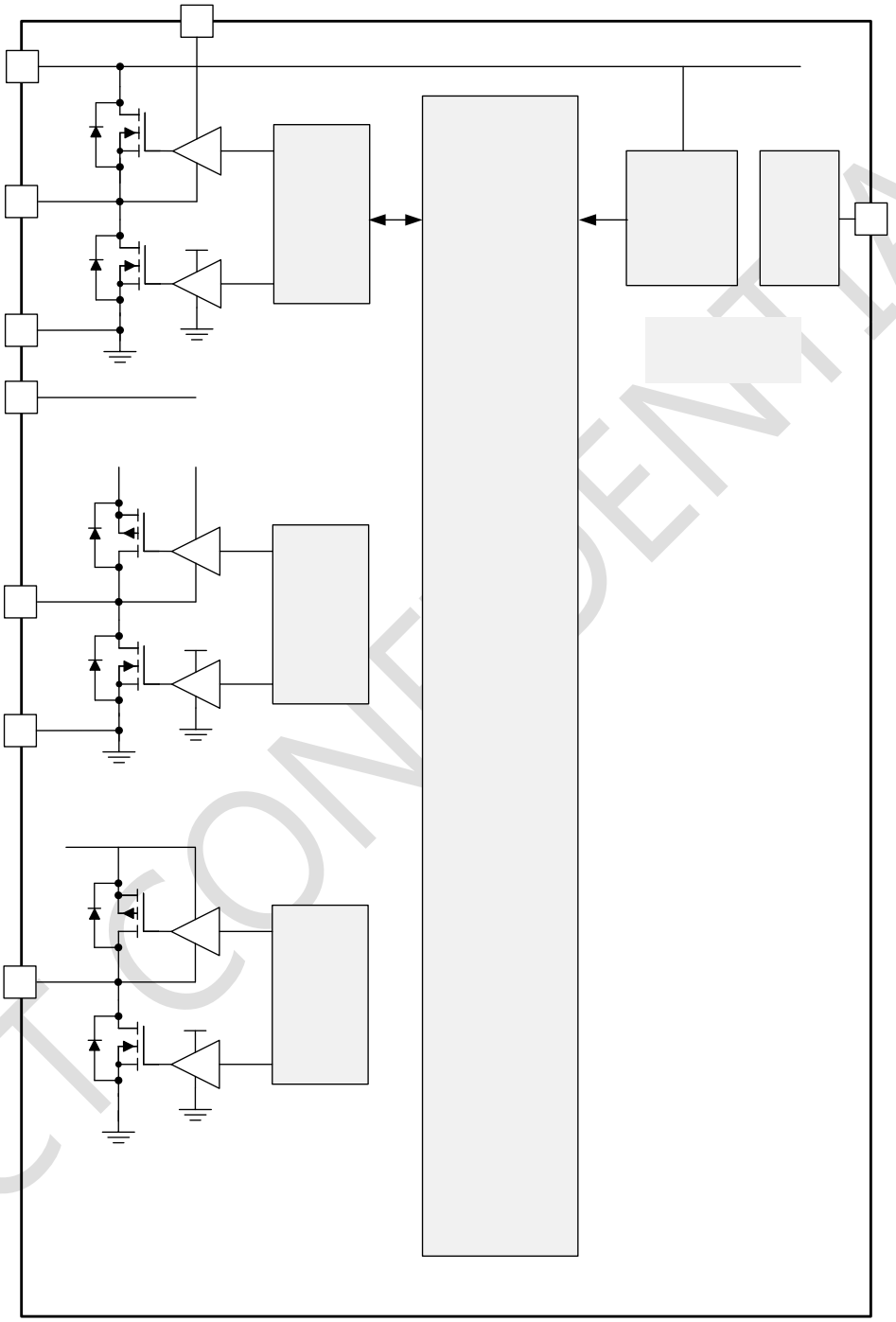
FUNCTIONAL BLOCK DIAGRAM



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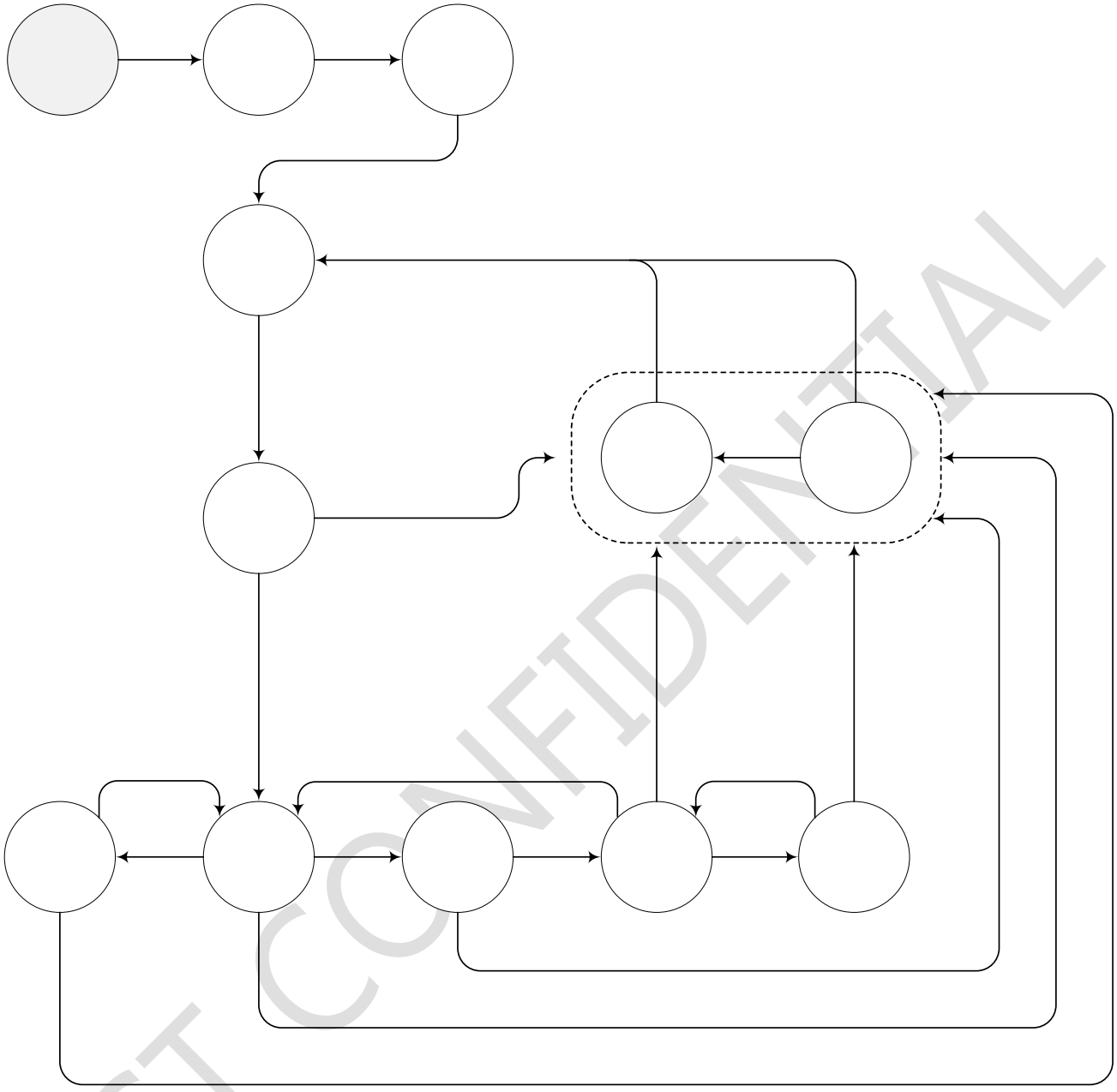

Figure 14. Operating State Machine and Transitions

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LOADOTP State

Once the device enters LOADOTP state, OTP data will be loaded into corresponding registers, then STANDBY state is entered.

STANDBY State

STANDBY state is where the device could be held on to check and wait for all conditions met to power up. To exit STANDBY state, VIN shall be higher than V_{IN_START} threshold, output rails shall be discharged and no other critical fault like thermal shutdown is triggered. The device will transit to POWERUP state almost immediately if all conditions are met when entering STANDBY state.

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RECOVER State

RECOVER state is an intermediate state when the device is awakened from SLEEP state. The channels disabled in SLEEP state will start up with the turn-on delay time same as in POWERUP state, and other channels will resume to FCCM operation. After all outputs are built up successfully, the device will enter NORMAL state. If any reset event triggered in RECOVER state, the device goes to RCVRST state.

RCVRST State

RCVRST state is an extra reset state to assert RESETB pin with output rails keep starting up in programmed sequence. This state aims to allow possible reset events to be triggered for those continuously enabled rails, like an output OV/UV. The device will go back to RECOVER state automatically once the hold time expired and the reset event discontinued.

TURNOFF State

If the device is manually turned off (e.g., writing **EN_ALL[0]**=0 online), or VIN drops to lower than V_{IN_STOP} threshold after start-up, TURNOFF state will be entered. All channels will be shut down with their turn-off delay time configuration in register **CONFIG_SEQ45** and **CONFIG_SEQ23**. See Figure 21 for a detailed power down sequence. After power down sequence is finished, the device will go back to STANDBY state waiting for reboot. If any deep safe event triggered in TURNOFF state, the device transits to DEEPSAFE state.

DEEPSAFE State

In DEEPSAFE state, all channels are shut off and RESETB pin is pulled low. Regardless of current state, the device can always jump to DEEPSAFE state when any of the deep safe events shown in Table 3 occurs after start-up. All power rails are shut down immediately and simultaneously while I2C interface keeps alive in DEEPSAFE state, allowing user to communicate with the device and read the status registers to locate the specific fault. The device will go back to STANDBY state once the hiccup timer expired and the deep safe event discontinued.

Table 3. Deep Safe Event

Category	Deep Safe Event	Status Bit
Analog	Buck1 output is out of deep OVP/UVP range or UV along with OC	DEEPOVP1[0], DEEPUVP1[0], UV1[0], OC1[0]
	Buck2 output is out of deep OVP/UVP range or UV along with OC	DEEPOVP2[0], DEEPUVP2[0], UV2[0], OC2[0]
	Buck3 output is out of deep OVP/UVP range or UV along with OC	DEEPOVP3[0], DEEPUVP3[0], UV3[0], OC3[0]
	LDO4 output is out of deep OVP/UVP range or UV along with OC	DEEPOVP4[0], DEEPUVP4[0], UV4[0], OC4[0]
	VMON deep OVP/UVP (when VMON_DEEPSAFE_CTRL[0]=0)	DEEPOVP5[0], DEEPUVP5[0],
	VIN OVP (when VINOVP_DEEPSAFE_CTRL[0]=0)	VIN_OVP[0]
	VCC OVP	VCC_OVP[0]
	Thermal shutdown	THSD[0]
Digital	ERRIN input high (when GPIO2 configured as ERRIN)	ERRIN[0]

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High Efficiency Regulators

All three buck converters employ 2.2MHz fixed frequency peak current mode control. Optional Forced Continuous Conduction Mode (FCCM) ensures good output performance at light-load, or Pulse Skip Mode (PSM) to provide excellent light-load efficiency. HV Buck1 is always the first one to power up, LV Buck2 and LV Buck3 then will start up with corresponding turn-on delay time configuration. The soft-start time is fixed at 0.8ms for all three buck converters.

Buck1 is a high-voltage synchronous buck converter directly powered from VIN pin. Buck1 output can be regulated at 2.7V to 5V with down to 100mV steps, providing a continuous output current of up to 2A. An external 100nF ceramic capacitor between BST and SW1 pins is required to power high-side power MOSFET gate driver, which is charged from VCC when low-side power MOSFET is on. Buck1 output is the power supply for other channels.

Buck2 and Buck3 are two identical low-voltage synchronous buck converter powered by Buck1. Both Buck2 and Buck3 output can be regulated at 0.6V to 2.15V with 50mV steps, providing up to 2A continuous output current. To further improve the EMI performance, Buck2 and Buck3 will operate in 180° phase shift.

LDO4 is a high PSRR, low noise LDO designed for analog power rail, also powered from Buck1. LDO4 output can be regulated at 1.6V to 3.5V with 50mV steps, providing a continuous output current of up to 300mA.

All output voltages are pre-programmed without any external feedback divider, and continuously monitored during operation. There is a two-stage OV/UV protection strategy. Any output OV/UV condition will trigger a reset event to pull RESETB pin low. For worse OV/UV cases, deep over-voltage protection or deep under-voltage protection will kick in to shut down all channels, as a deep safe event.

Deep Over-voltage Protection

If any output voltage exceeds the deep over-voltage protection threshold configured in **DEEP_OVP_SEL[1:0]** during operation, a deep safe event is triggered and all outputs will be shut down for the hiccup time. In this hiccup time, all output rails will be discharged by internal circuit. When the hiccup timer expired and the deep over-voltage condition discontinued, the device will start up again with configured power up sequence.

Deep Under-voltage Protection

If any output voltage falls below the deep under-voltage protection threshold configured in **DEEP_UVP_SEL[1:0]** during operation, a deep safe event is triggered and all outputs will be shut down for the hiccup time. In this hiccup time, all output rails will be discharged by internal circuit. When the hiccup timer expired and the deep under-voltage condition discontinued, the device will start up again with configured power up sequence.

Over Current Protection

The buck converters implement over current protection with cycle-by-cycle limit for both high-side power MOSFET peak current and low-side power MOSFET valley current to avoid inductor current running away during unexpected overload or output short-circuit. When the converter is not able to provide enough output current to meet loading requirement with the inductor current already clamped at the over current limit, the output voltage drops below the regulation target. If the peak current limit is kicked for continuous 32 times and the output voltage is below its UV threshold, the converter will stop switching and the device will transit to DEEPSAFE state. After a hiccup time, the device will try to restart again, but transit to DEEPSAFE state again if over-load condition not removed. The hiccup protection mode greatly reduces the average short-circuit current to alleviate thermal issues and protect the device. Once over-load condition removed, the device would recover to normal operation in NORMAL state.

For LDO4, if the load current is higher than its current limit, the output voltage will start to drop and the input current will be clamped at the current limit. Then the output under-voltage or deep under-voltage protection would be triggered if the over-load condition continued.

Thermal Shutdown

The thermal shutdown protects the device from damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 155°C, the status bit **THWR[0]** will be set as a high temperature warning flag while the device keeps in normal operation. If the junction temperature continues to rise and exceeds 175°C,

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thermal shutdown as a deep safe event will be triggered and the status bit **THSD[0]** will be set. The device will shut down all channels immediately and transit to DEEPSAFE state. After the hiccup timer expired, the device will try to restart if the over-temperature condition discontinued.

Status Bits

The SCT61242Q provides 6 status registers, **STATUS1~6**, to record all kinds of warnings, errors or faults during operation. Once being set, these status bits will not be reset until VCC under-voltage (e.g., VIN power off), or manually writing '1' to clear corresponding status bit via I2C. When GPIO2 is configured as INTB, any status bits being set will pull INTB low as an indicator to notify other devices. INTB level keeps latched after pulled low and only reset to high until all status bits are cleared. Some fault conditions could be masked for INTB through register **CTRL_FLTMAP2**.

Frequency Spread Spectrum

To meet CISPR and automotive EMI compliance, the SCT61242Q implements optional Frequency Spread Spectrum (FSS) function. The FSS circuitry shifts the 2.2MHz switching frequency in ±4/±8%

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Table 4. GPIO Configuration

Pin	I/O	Function	Description
	Input	VMON	External voltage monitor input. VMON can be used to monitor the external regulator output voltage with configurable activation timing. Any VMON OV/UV condition will trigger a reset event and VMON deep OVP/UVP will trigg a MON Anyt VMvWnd 6]T
GPIO1			

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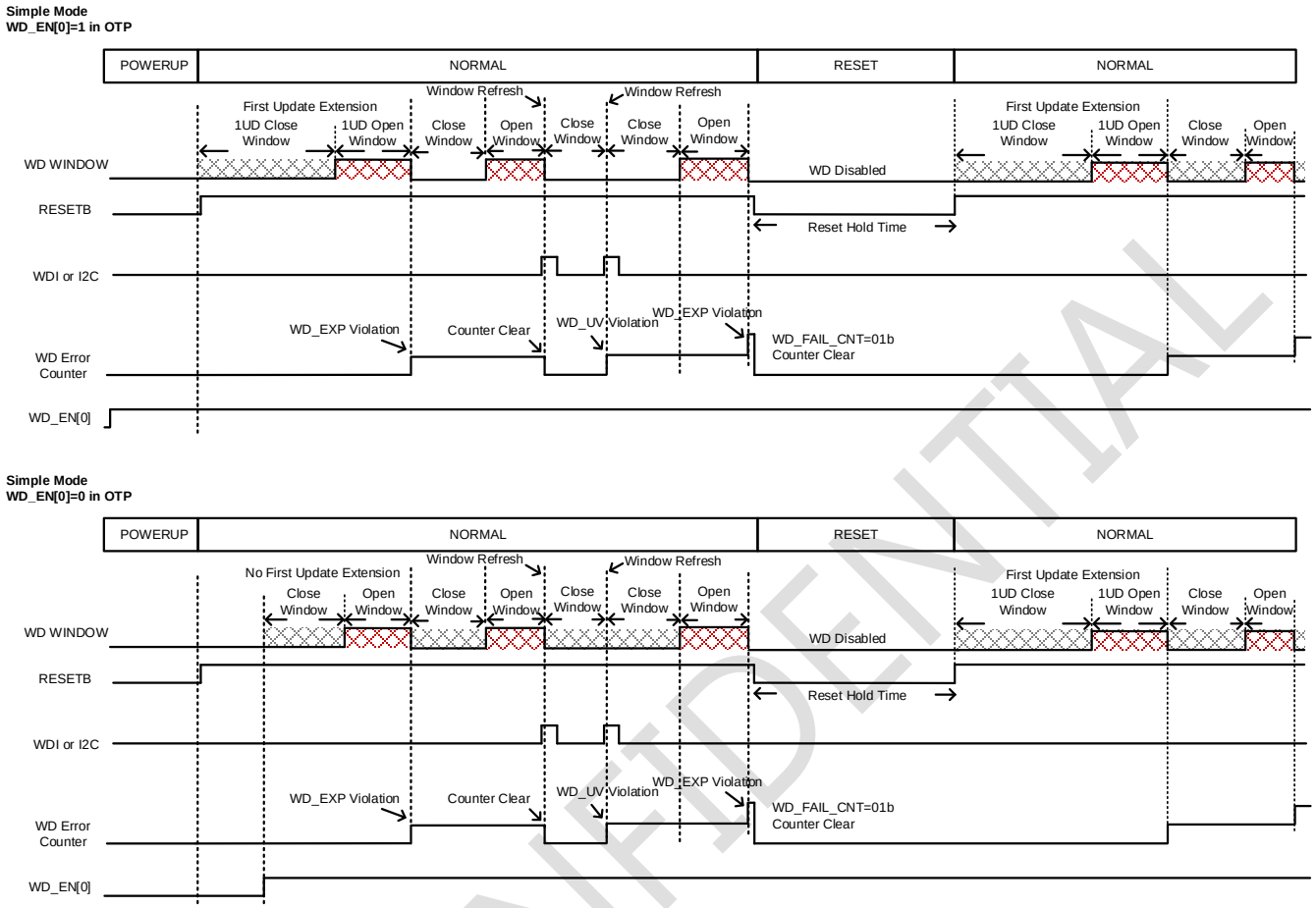

Figure 15. Simple Watchdog Operation and Timing

In QA watchdog mode, watchdog is fed by writing specific value to register **WD_KEY** and the operation is similar to simple watchdog mode. Once the device enters NORMAL state, the watchdog will be activated starting by close window and followed by open window, with extension cycles configured by **WD_1UD[0]**. The duration of close window and open window in each cycle could be configured by **WD_TCLOSE[3:0]** and **WD_TOPEN[3:0]**, and watchdog shall be fed only within open window. The correct value written to register **WD_KEY** shall be the same as the current value in **WD_KEY**, which can also be calculated with the previous value in **WD_KEY** by a LFSR polynomial of x8 + x6 + x5 + x4 + 1. A correct watchdog feed action will restart the whole window cycle immediately. If an incorrect value is written, status bit **WD_LFSR[0]** will be set, the watchdog error counter will be incremented and the window cycle will also be refreshed. If watchdog fed during close window, status bit **WD_UV[0]** will be set, the watchdog error counter will be incremented and the window cycle will be refreshed. Any feed action during the first close window after NORMAL state entered will be blanked. If watchdog not fed before open window expired, status bit **WD_EXP[0]** will be set, the watchdog error counter will be incremented and the window cycle will be refreshed. When watchdog error counter reaches the times configured in **WD_FAIL_CNT[1:0]**, a reset event will be triggered and status bit **WD_ERR[0]** will be set. The device transits to RESET state and goes back to NORMAL state after a hold time. The watchdog error counter is reset and watchdog window cycle is initiated when transiting from RESET back to NORMAL state.

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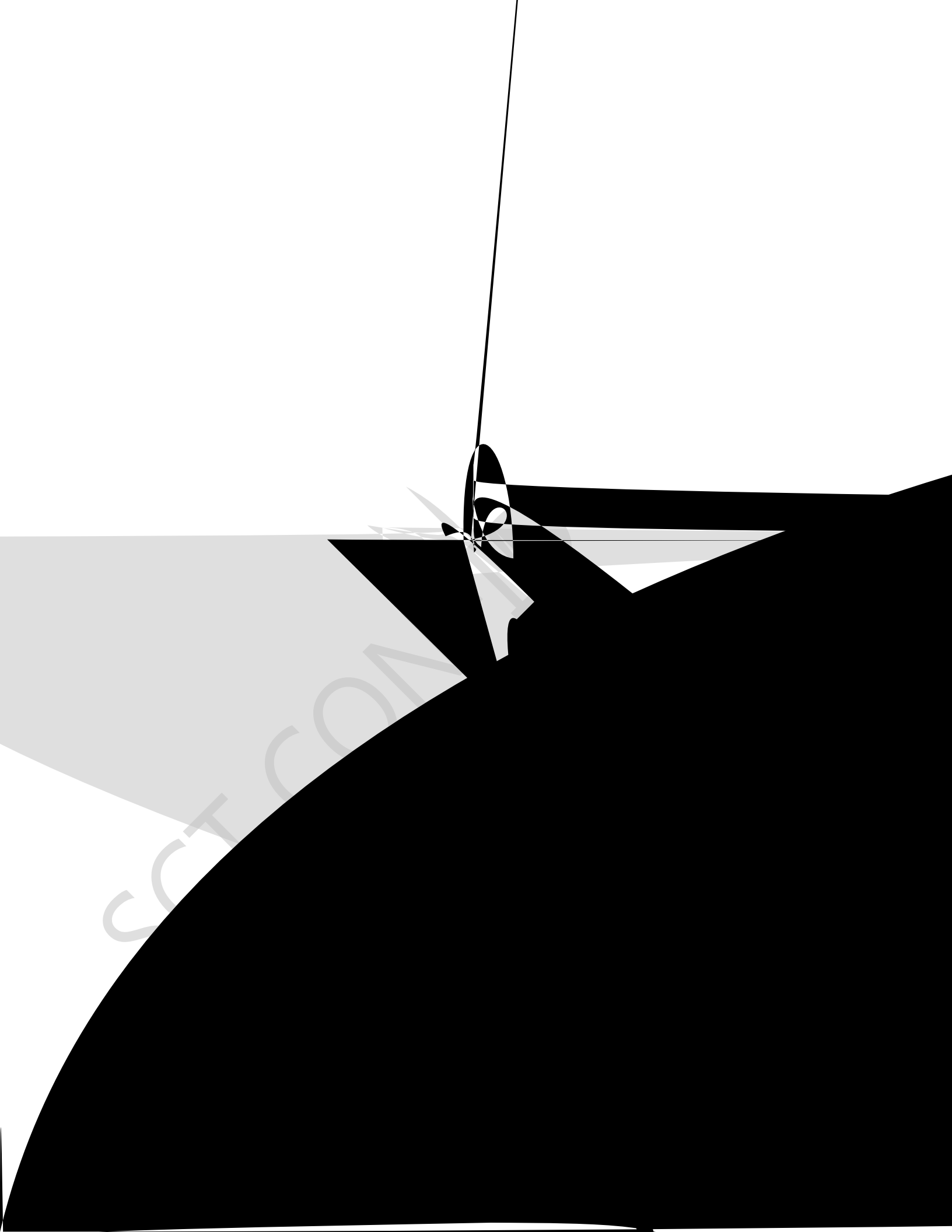
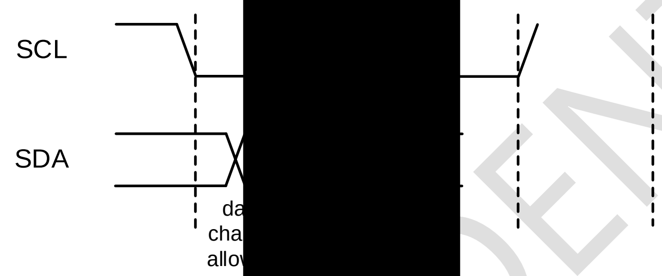


I2C Interface

The SCT61242Q integrates a two-wire serial in[redacted]onal communications between the device and the master through the bus. The I2C protocol defin[redacted]he serial data line (SDA) and the serial clock line (SCL). The SCT61242Q is assigned with a u[redacted]s 0x38 by default and operates as a slaver. The master drives the SCL line and transfer bidirec[redacted] SDA line. Both the SCL and the SDA lines need a pull-up resistor connected to bus voltage sin[redacted] default state when bus is idle. The SCT61242Q supports Standard mode (up to 100kHz), Fast-[redacted]z) and Fast-mode Plus (up to 1MHz). The internal filtering ignores spikes and noises on the bus li[redacted]a integrity. The maximum capacitive load for each bus line is given in Electrical Characteristic thu[redacted]terfaces is limited.

Data Validity

The data on the SDA line must be stable durin[redacted]f the clock. The high or low state of the data line can only change when the clock signal on the [redacted]ET304090542 y -8 - 412 70.90 566.62 d3A65T90542[.to



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Packet Error Checking (PEC)

The SCT61242Q supports optional packet error checking (PEC) byte during the I2C communication. PEC can significantly increase fault coverage on the I2C interface. The PEC byte is implemented through CRC-8 polynomial of x8 + x2 + x +1. The PEC byte does not take ACK, NACK, START, STOP, Repeated START bits into calculation. The PEC byte is calculated with the register address and data byte over the entire message from the first START condition. Note that the slave address is not involved in the calculation both in write and read command. When PEC is enabled, the device will reject the write command if the master send an incorrect PEC byte. When in read mode with PEC enabled, the master should acknowledge the data byte thus then the device will send the PEC byte. PEC function can be enabled or disabled by **PEC_EN[0]**.

Write Data Format

A write to the device includes transmission of the following:

- START condition
- Slave address with the write bit set to 0
- 1 byte of data to register address
- 1 byte of data to the command register
- STOP condition

Read Data Format

A read from the device includes the following:

- Transmission of a START condition
- Slave address with the write bit set to 0
- 1 byte of data to register address
- Restart condition
- Slave address with read bit set to 1
- 1 byte of data to the command register
- STOP condition

Figure 19 illustrates the proper format for one frame.

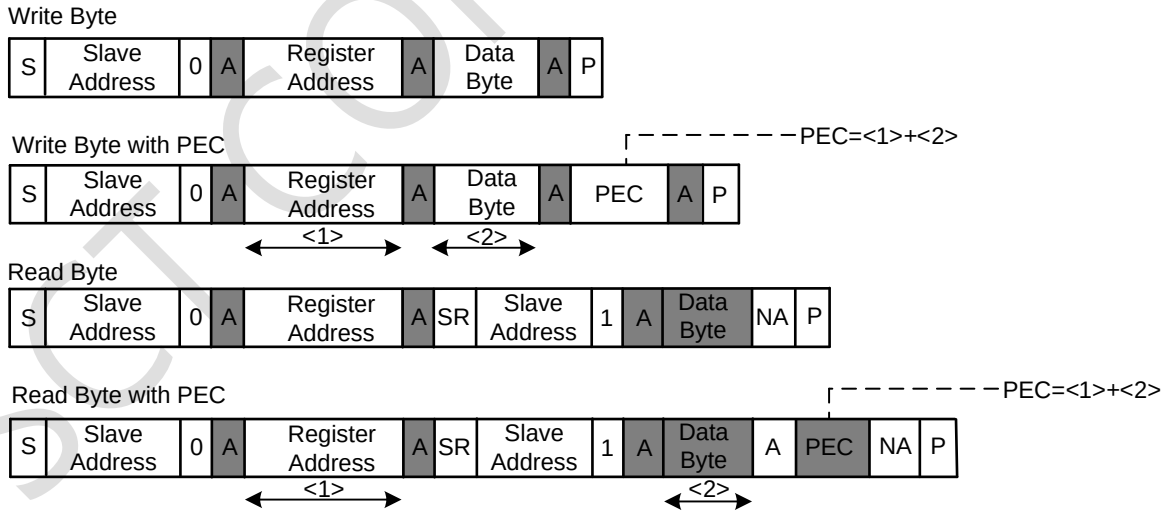

Figure 19. Transmission Data Format

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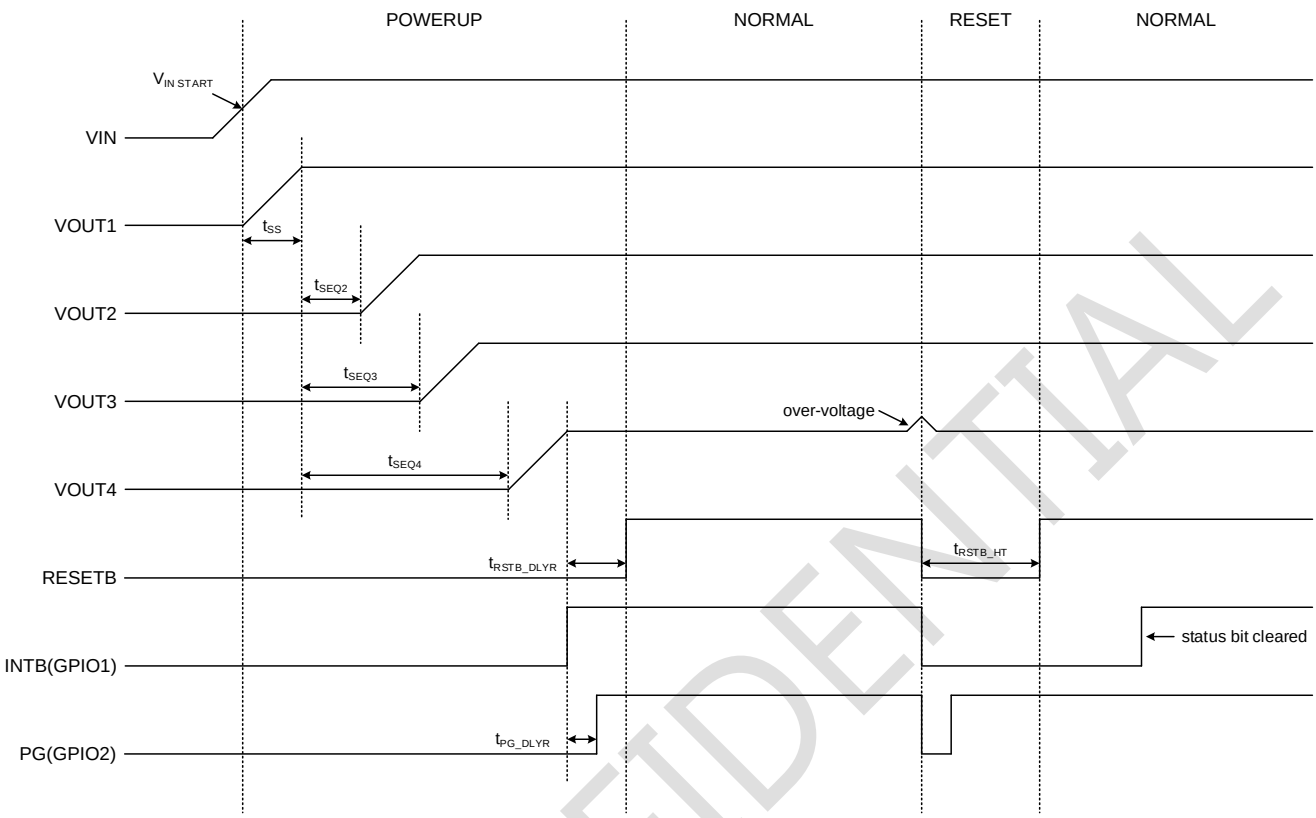

Figure 20. Power Up Sequence

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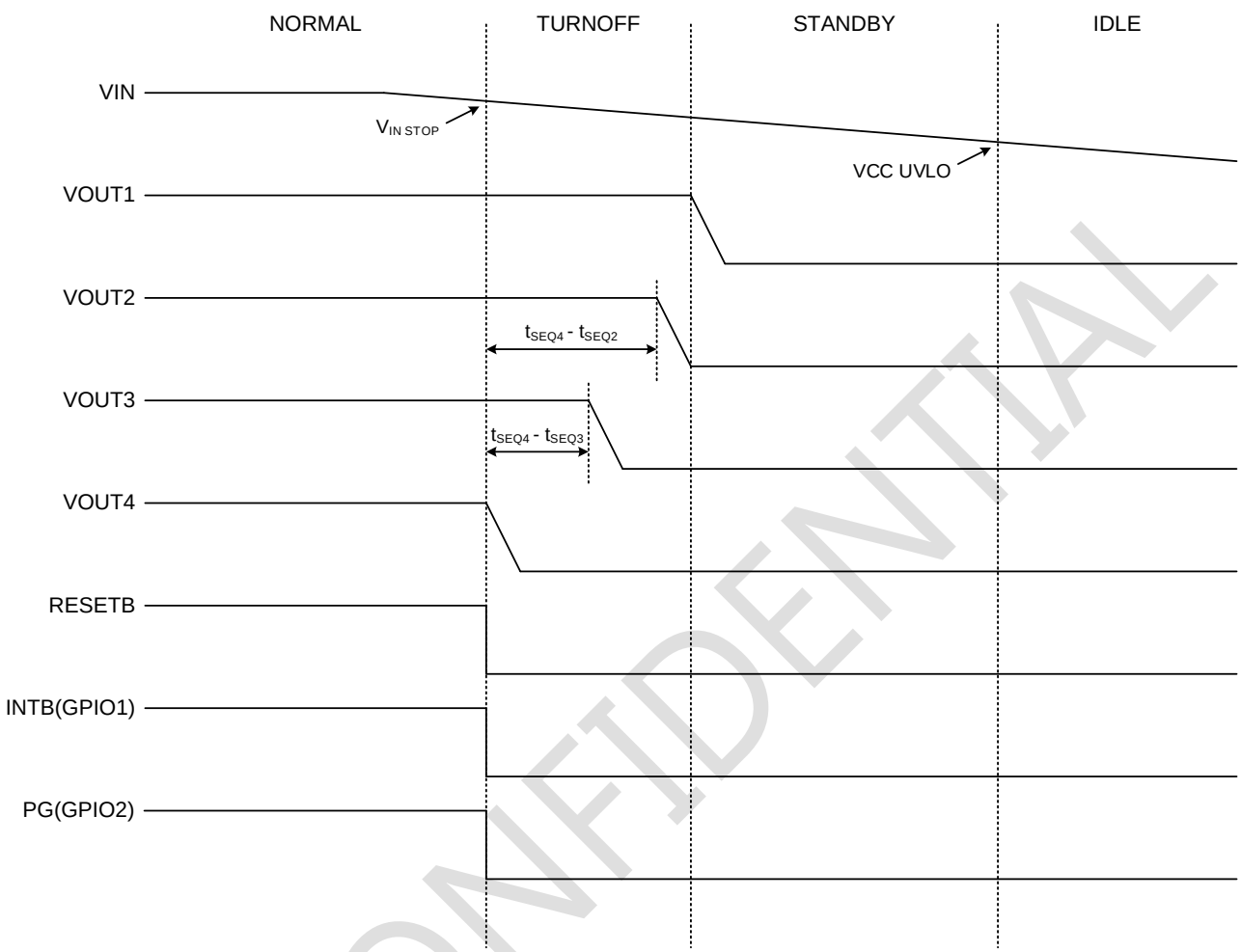

Figure 21. Power Down Sequence

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APPLICATION INFORMATION

Typical Application

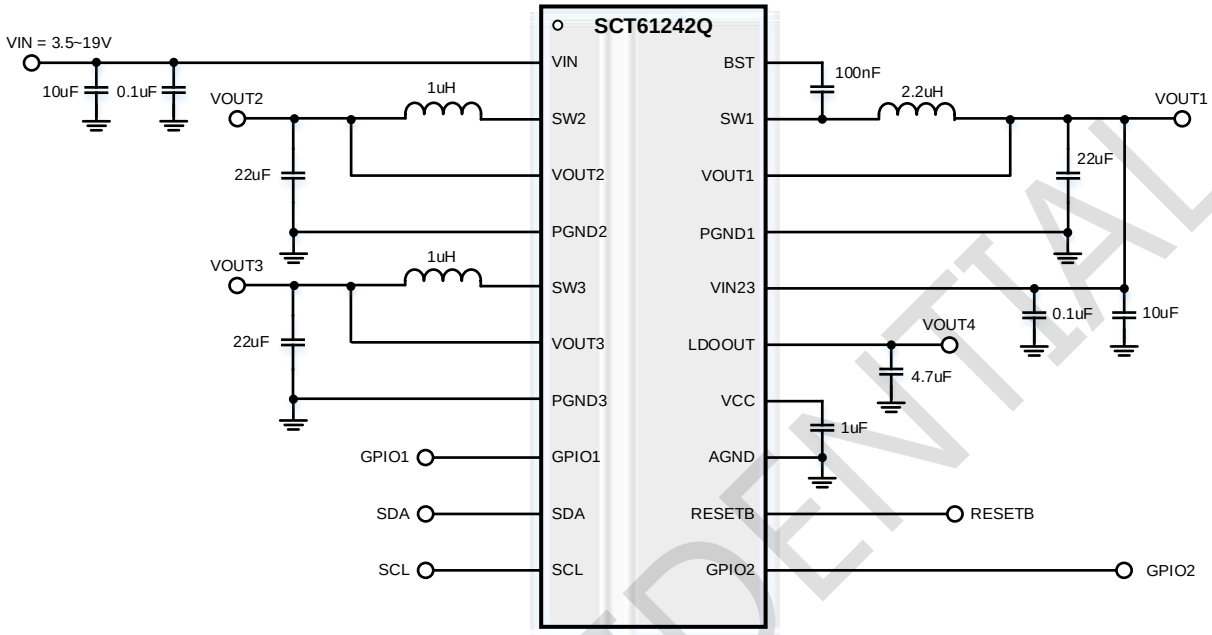

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Table 6. Recommended BOM for Typical Application

Output Rail	Switching Frequency	Inductor	Output Capacitor
Buck1	2.2MHz	2.2uH	10uF or 22uF
Buck2	2.2MHz	1uH	10uF or 22uF
Buck3	2.2MHz	1uH	10uF or 22uF
LDO4	-	-	4.7uF

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Application Waveforms

V_{IN} = 10V, V_{OUT1} = 3.3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{OUT4} = 2.8V, L1 = 2.2uH, L2 = L3 = 1uH, FCCM, T_A = 25°C, unless otherwise noted.

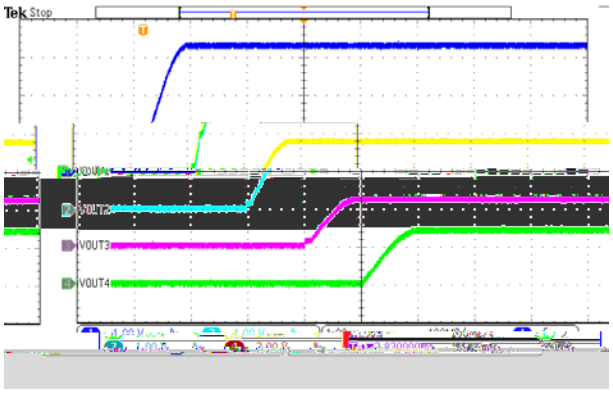

Figure 24. Power Up Sequence

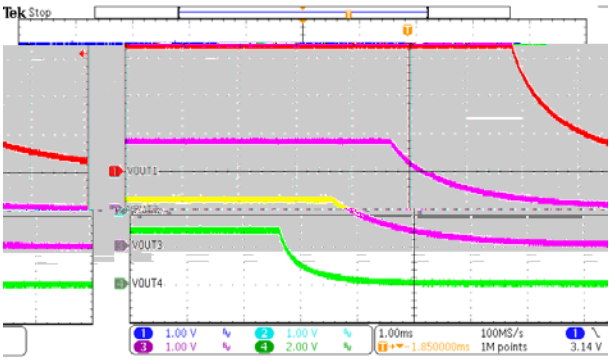

Figure 25. Power Down Sequence

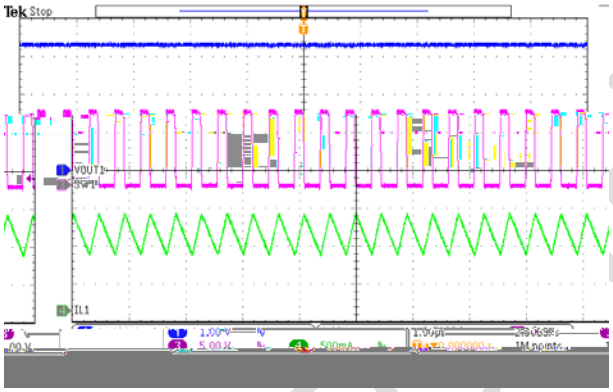

Figure 26. Buck1 Steady State, Load=1A

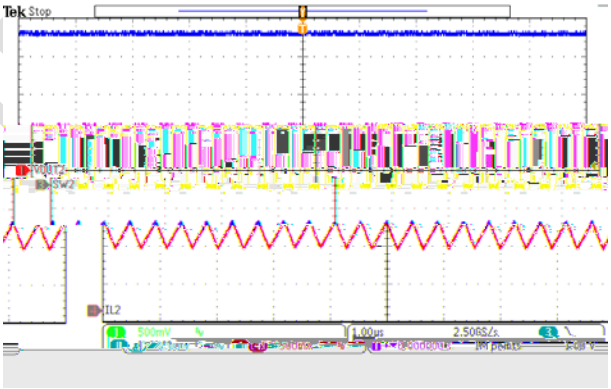

Figure 27. Buck2 Steady State, Load=1A

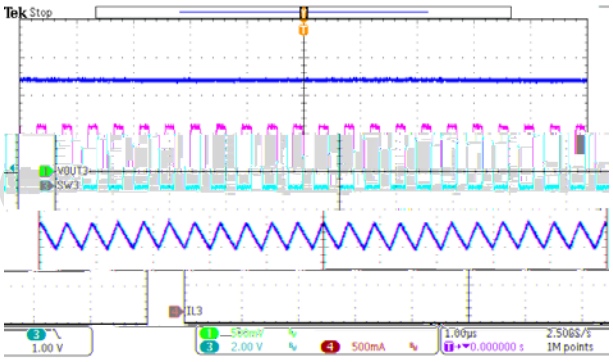

Figure 28. Buck3 Steady State, Load=1A

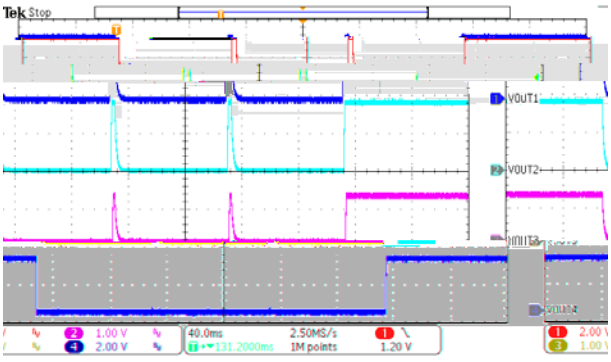

Figure 29. LDO4 Short-circuit and Recovery

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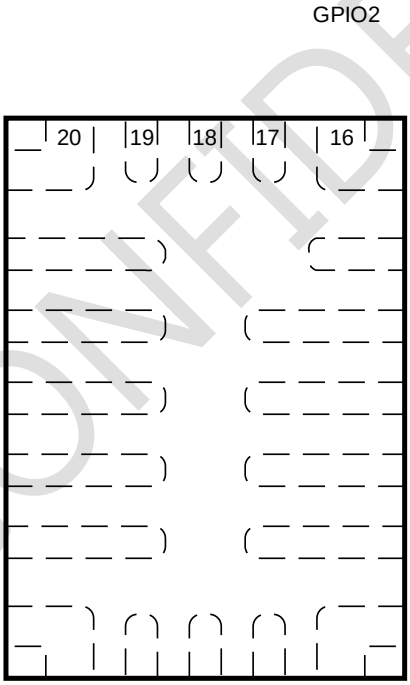
Layout Guideline

Proper PCB layout is a critical for device's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The rule of thumb is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over-heat area.
2. Place a low ESR ceramic capacitor as close to VIN and VIN23 pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.
4. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias.
5. Output inductor should be placed close to the SW pin. The switching area of the PCB conductor minimized to prevent excessive capacitive coupling.
6. Connect AGND to PGND plane at a single point.



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CTRL_ENLP [7:0]			
ADDRESS: 0x02			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:4]	RESERVED	R	/
[3]	OFF4_LP	W/R	LDO4 control for low power mode. 0: LDO4 will stay alive in low power mode. 1: LDO4 will be turned off in low power mode.
[2]	OFF3_LP	W/R	LV Buck3 control for low power mode. 0: LV Buck3 will stay alive in low power mode. 1: LV Buck3 will be turned off in low power mode.
[1]	OFF2_LP	W/R	LV Buck2 control for low power mode. 0: LV Buck2 will stay alive in low power mode. 1: LV Buck2 will be turned off in low power mode.
[0]	EN_LP	W/R	Enable for low power mode. This bit will be self-cleared when exiting SLEEP

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CONFIG_BUCK1 [7:0]			
ADDRESS: 0x04			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	PSM1	R	Buck1 FCCM/PSM mode selection in NORMAL state. 0: FCCM 1: PSM
[6:4]	RESERVED	R	/
[3:0]	VOUT1	R	Buck1 output voltage setting.

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CONFIG_BUCK3 [7:0]			
ADDRESS: 0x06			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	PSM3	R	Buck3 FCCM/PSM mode selection in NORMAL state. 0: FCCM 1: PSM
[6:5]	RESERVED	R	/
[4:0]	VOUT3	R	Buck3 output voltage setting. 00000: 0.6V 00001: 0.65V 00010: 0.7V … 01100: 1.2V … 11000: 1.8V … 11110: 2.1V 11111: 2.15V (V_{OUT3} = 0.6V + VOUT3[4:0] × 0.05V)

CONFIG_LDO4 [7:0]			
ADDRESS: 0x07			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:5]	RESERVED	R	/
[4:0]	VOUT4	R	LDO4 output voltage setting. 00000: 1.6V 00001: 1.65V 00010: 1.7V … 01001: 2.05V 01010: 2.1V (50mV step from 1.6V to 2.1V, V_{OUT4} = 1.6V + VOUT4[4:0] × 0.05V) 01011: 2.5V 01100: 2.55V … 10001: 2.8V … 11011: 3.3V … 11110: 3.45V 11111: 3.5V (50mV step from 2.5V to 3.5V, V_{OUT4} = 2.5V + VOUT4[4:0] × 0.05V)

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CONFIG_VMON [7:0]			
ADDRESS: 0x08			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:5]	RESERVED	R	/
[4:0]	VMON	R	VMON monitor voltage setting. 00000: 0.6V 00001: 0.65V 00010: 0.7V … 11110: 2.1V 11111: 2.15V (V_{MON} = 0.6V + VMON[4:0] × 0.05V)

CONFIG_MISC [7:0]			
ADDRESS: 0x09			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:6]	DEEP_OVP_SEL	R	Deep OVP threshold selection for all channels. 00: 115% 01: 112% 10: 110% 11: 108%
[5:4]	DEEP_UVP_SEL	R	Deep UVP threshold selection for all channels. 00: 75% 01: 80% 10: 85% 11: 90%
[3]	VINOVP_DEEPSAFE_CTRL	R	VIN OVP action selection. 0: Enter DEEPSAFE state 1: Enter RESET state
[2]	VMON_DEEPSAFE_CTRL	R	VMON deep OVP/UVP action selection. 0: Enter DEEPSAFE state 1: Enter RESET state
[1:0]	VMON_BLANK	R	VMON monitor blanking time. VMON pin will be monitored after this blanking time since SEQOUT pulled high. If SEQOUT is not used, the blanking time starts from SEQ5[3:0] configured timing. 00: 1ms 01: 2ms 10: 4ms 11: 8ms

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CONFIG_T1 [7:0]			
ADDRESS: 0x0A			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:6]	RESETB_HT	R	RESETB assertion low-level hold time. The RESETB pin is pulled low at least for this duration when any reset event triggered. After the hold time expired, NORMAL state will be entered if the reset event discontinued. 00: 10ms 01: 20ms 10: 30ms 11: 40ms
[5:4]	RESETB_DLYR	R	RESETB rising delay time after all channels are built up in POWERUP state. When RESETB_DLYR_SCALE[0]=0: 00: 0.5ms 01: 1ms 10: 2ms 11: 4ms When RESETB_DLYR_SCALE[0]=1: 00: 2.5ms 01: 5ms 10: 10ms 11: 20ms
[3:2]	PG_DLYR	R	PG rising delay time when GPIO2 is set to PG. 00: 50us 01: 100us 10: 150us 11: 200us
[1:0]	PG_DLYF	R	PG falling delay time when GPIO2 is set to PG. 00: 50us 01: 100us 10: 150us 11: 200us

CONFIG_T2 [7:0]			
ADDRESS: 0x0B			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:6]	ON_DELAY_SCALE	R	Power up sequence on delay time scale selection. 00: t_{ON_SCALE} = 0.5ms (0~7.5ms range) 01: t_{ON_SCALE} = 1ms (0~15ms range) 10: t_{ON_SCALE} = 2ms (0~30ms range) 11: t_{ON_SCALE} = 4ms (0~60ms range)
[5:4]	OFF_DELAY_SCALE	R	Power down sequence off delay time scale selection. 00: t_{OFF_SCALE} = 0.5ms (0~7.5ms range) 01: t_{OFF_SCALE} = 1ms (0~15ms range) 10: t_{OFF_SCALE} = 2ms (0~30ms range) 11: t_{OFF_SCALE} = 4ms (0~60ms range)
[3:0]	OVUV_FILTER_TIME	R	OV rising/UV falling filter time for all output comparators. t_{FILT} = (OVUV_FILTER_TIME[3:0] + 1) × 10us

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CONFIG_WD1 [7:0]			
ADDRESS: 0x0E			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	WD_MODE	W/R	Watchdog mode selection. 0: QA watchdog 1: Simple watchdog
[6]	WD_SCALE	W/R	Watchdog clock divider scale. 0: t_{WDCLK_SCALE} = 128us 1: t_{WDCLK_SCALE} = 8192us
[5:0]	WD_CLK	W/R	Watchdog clock divider. t_{WDCLK} = (WD_CLK[5:0] + 1) × t_{WDCLK_SCALE}

CONFIG_WD2 [7:0]			
ADDRESS: 0x0F			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:4]	WD_TCLOSE	W/R	Watchdog close window duration time configuration. Feeding watchdog in close window will trigger a WD_UV violation and increase watchdog error counter by 1. t_{WD_CLOSE} = (WD_TCLOSE[3:0] + 1) × 8 × t_{WDCLK}
[3:0]	WD_TOPEN	W/R	Watchdog open window duration time configuration. Feeding watchdog correctly in open window will restart the whole window cycle immediately. t_{WD_OPEN} = (WD_TOPEN[3:0] + 1) × 8 × t_{WDCLK}

CONFIG_WD3 [7:0]			
ADDRESS: 0x10			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:6]	RESERVED	R	/
[5:4]	WD_FAIL_CNT	W/R	Watchdog error counting times configuration. When watchdog error counter reaches this number, a RESET event will be triggered. 00: 1 time 01: 2 times 10: 3 times 11: 4 times
[3]	WD_EN	W/R	Watchdog enable. 0: Disabled 1: Enabled
[2:0]	WD_1UD	W/R	Watchdog first update extension. This configures the extra length of the first open/close window after entering NORMAL state. $t_{WD\_CLOSE\_1st}$ = (WD_1UD[2:0] + 1) × t_{WD_CLOSE} $t_{WD\_OPEN\_1st}$ = (WD_1UD[2:0] + 1) × t_{WD_OPEN}

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WD_KEY [7:0]			
ADDRESS: 0x11			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:0]	WD_KEY	W/R	Watchdog key. The current key can be read from this register and the next key will be updated after the current key written to this register by user. For simple watchdog, writing any value to the WD_KEY register will refresh the watchdog and the value written will be ignored. For QA watchdog, writing the correct value to the WD_KEY register during an open window will result in a window refresh and the WD_KEY register being updated. Writing the incorrect value to the WD_KEY register during an open window will result in a WD_LFSR violation. Writing any value during a closed window will result in a WD_UV violation. LFSR polynomial: x8 + x6 + x5 + x4 + 1

WD_LOCK [7:0]			
ADDRESS: 0x12			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:0]	WD_LOCK	W/R	Watchdog configuration lock protection. AAh: Watchdog configuration registers (CONFIG_WD1/2/3) are writeable. Others: Watchdog configuration registers (CONFIG_WD1/2/3) are read-only.

CONFIG_GPIO0 [7:0]			
ADDRESS: 0x13			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	RESETB_DLYR_SCALE	R	RESETB rising delay time scale selection. 0: t_{RST_SCALE} = 0.5ms (0.5~4ms range) 1: t_{RST_SCALE} = 2.5ms (2.5~20ms range)
[6]	RESERVED	R	/
[5:4]	GPIO2_BLANK	R	GPIO2 input signal blanking time after RESETB pulled high. 00: 0ms 01: 2.5ms 10: 5ms 11: 10ms
[3:2]	GPIO2_DLYR	R	GPIO2 input signal rising deglitch time. 00: 80us 01: 40us 10: 20us 11: 10us
[1:0]	GPIO2_DLYF	R	GPIO2 input signal falling deglitch time. 00: 80us 01: 40us 10: 20us 11: 10us

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CONFIG_GPIO1 [7:0]			
ADDRESS: 0x14			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	VIO	R	High level voltage selection when RESETB/GPIO1/GPIO2 configured as push-pull output. 0: 3.3V 1: 1.8V
[6]	RESETB_OUT	R	RESETB output configuration. 0: Open-drain 1: Push-pull
[5]	GPIO1_OUT	R	GPIO1 output configuration. 0: Open-drain 1: Push-pull
[4]	GPIO2_OUT	R	GPIO2 output configuration. 0: Open-drain 1: Push-pull
[3]	GPIO1_SEL	R	GPIO1 function selection. 0: INTB (output) 1: VMON (analog input)
[2:0]	GPIO2_SEL	R	GPIO2 function selection. 000: SEQOUT (output) 001: PG (output) 010: GPO (output) 011: INTB (output) 100: ERRIN (digital input) 101: WDI (digital input) 110: SLEEPB (digital input) 111: RSTIN (digital input)

CTRL_GPO [7:0]			
ADDRESS: 0x15			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:1]	RESERVED	R	/
[0]	CTRL_GPIO	W/R	GPIO2 output state when GPIO2 configured as GPO. 0: Low 1: High

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CTRL_FLTMAP2 [7:0]			
ADDRESS: 0x17			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	RSTMAP_RSTIN	W/R	Reset event and RESETB pin mapping for RSTIN. 0: Not mapped to reset event and RESETB pin 1: Mapped to reset event and RESETB pin
[6]	RSTMAP_VMONDP	W/R	Reset event and RESETB pin mapping for VMON deep OVP/UVP when VMON_DEEPSAFE_CTRL[0]=1. 0: Not mapped to reset event and RESETB pin 1: Mapped to reset event and RESETB pin
[5]	RESERVED	R	/
[4]	INTBMAP_I2C	W/R	INTB pin mapping for I2C PEC error. 0: Not mapped to INTB pin 1: Mapped to INTB pin
[3]	INTBMAP_THWR	W/R	INTB pin mapping for thermal warning. 0: Not mapped to INTB pin 1: Mapped to INTB pin
[2]	RESERVED	R	/
[1]	INTBMAP_WD	W/R	INTB pin mapping for watchdog error (WD_ERR, WD_LFSR, WD_UV, WD_EXP). 0: Not mapped to INTB pin 1: Mapped to INTB pin
[0]	STATEMAP_ERRIN	W/R	State machine mapping for ERRIN. 0: Not mapped to state machine 1: Mapped to state machine

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STATUS1 [7:0]			
ADDRESS: 0x18			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	UV5	W1C/R	VMON under-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[6]	UV4	W1C/R	LDO4 output under-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[5]	UV3	W1C/R	Buck3 output under-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[4]	UV2	W1C/R	Buck2 output under-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[3]	UV1	W1C/R	Buck1 output under-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[2]	OV5	W1C/R	VMON over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[1]	OV4	W1C/R	LDO4 output over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[0]	OV3	W1C/R	Buck3 output over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.

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