19V Vin Quad Channel Power Management IC for Automotive Applications

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
- Wide Input Voltage Range: 4V-19V
- Synchronous HV Pre-Buck1:
  - Up to 1.2A Continuous Output Current
  - Auto-adaptive Output Voltage Depends on LDO Output Voltage
- Synchronous LV Post-Buck2:
  - Powered by Pre-Buck1
  - Up to 0.6A Continuous Output Current
  - Fixed Output Voltage of 1.8V
- Synchronous LV Post-Buck3:
  - Powered by Pre-Buck1
  - Up to 1.2A Continuous Output Current
  - Adjustable Output Voltage: 1.1V/1.2V/1.3V/1.5V
- LV Post-LDO:
  - Powered by Pre-Buck1
  - Up to 0.3A Continuous Output Current
  - Adjustable Output Voltage: 2.7V/2.8V/2.9V/3.3V
  - Low Noise and High PSRR
- Low Shutdown Current: 1uA
- Fixed 2.2MHz Switching Frequency
- Integrated Frequency Dither for EMI Mitigation
- FCCM Operation
- 60ns Minimum On-time
- 6 Flexible Sequence via External Resistor
- 9 Flexible Output Voltage via External Resistor
- Push-pull Power Good Indicator
- Integrated Hiccup Mode Protection Features:
  - Input Over-voltage Protection
  - Output Over-voltage Protection
  - Output Under-voltage Protection
  - Over-current Protection
  - Adjustable Under-voltage Lockout
  - Thermal Shutdown Protection
- Available in QFN-18L(2.5mm*3.5mm)

APPLICATIONS

- ADAS
- Compact Camera Module
- Cabin Monitor

DESCRIPTION

The SCT61240Q is a highly integrated power management IC (PMIC) optimized for automotive camera system. It integrates three high efficiency synchronous BUCK converters (HVBUCK1, LVBUCK2, LVBUCK3), and a high-PSRR low noise LDO with OV/UV monitoring on all outputs.

VOUT1 is the output of BUCK1, which is powered from VIN (Power Over Coax) and can output 1.2A continuous current with the output voltage set to LDOOUT+300mV/500mV or fixed 3.3V.

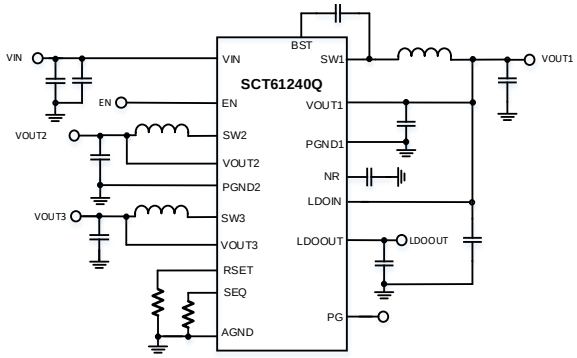
VOUT2 is the output of BUCK2, which is powered from VOUT1 and can output 600mA continuous current with the output voltage fixed to 1.8V.

VOUT3 is the output of BUCK3, which is powered from VOUT1 and can output 1.2A continuous current with the output voltage set to 1.1V/1.2V/1.3V/1.5V through RSET PIN for different sensors.

LDOOUT is the output of LDO, which is powered from VOUT1 (need to connect LDOIN to VOUT1) and can output 300mA continuous current with the output voltage set to 2.7V/2.8V/2.9V/3.3V through RSET PIN for different sensors.

With a compact QFN2.5x3.5 package, the SCT61240Q greatly reduces external components count and PCB space.

TYPICAL APPLICATION



REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version

Revision 1.0: Released to Market

Revision 1.1: Update DEVICE ORDER INFORMATION

Revision 1.2: Corrected few typographical errors.

Revision 1.3: Update DEVICE ORDER INFORMATION.

DEVICE ORDER INFORMATION

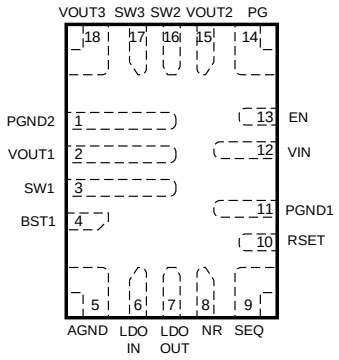
PART NUMBER	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	VOUT1	PG VOLTAGE	SOFT START	PACKAGE DESCRIPTION	MSL
SCT61240QFJCR	Tape & Reel	5000	1240Q	18	Fixed 3.3V	3.3V	0.4ms	FCTQFN 2.5X3.5-18L	1
SCT61240Q-0000FJCR	Tape & Reel	5000	1240Q	18	LDOOUT+0.3V	1.8V	0.4ms	FCTQFN 2.5X3.5-18L	1
SCT61240Q-0001FJCR	Tape & Reel	5000	1240Q	18	LDOOUT+0.5V	1.8V	0.4ms	FCTQFN 2.5X3.5-18L	1
SCT61240Q-0002FJCR	Tape & Reel	5000	1240Q	18	LDOOUT+0.5V	1.8V	1.6ms	FCTQFN 2.5X3.5-18L	1
SCT61240Q-0003FJCR	Tape & Reel	5000	1240Q	18	Fixed 3.3V	3.3V	0.4ms	FCTQFN 2.5X3.5-18L	1

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN, EN	-0.3	24	V
SW1	-0.3 (-1 in 30ns)	24	V
BST-SW1	-0.3	6	V
Others	-0.3	6	V
Junction temperature(2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

PIN CONFIGURATION



Top View: 18-Lead FCTQFN 2.5mmx3.5mm

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 170°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	DESCRIPTION
PGND2	1	Power ground for Buck 2 and Buck 3. Should be electrically connected to the system power ground plane with the shortest and lowest-impedance connection possible.
VOUT1	2	Feedback for Buck 1 and power source for Buck 2 and Buck 3. Connect VOUT1 pin to the buck 1 output directly. A decoupling capacitor to ground is recommended to be placed close to VOUT1 to minimize switching spikes.
SW1	3	Buck 1 switch node. SW is the output of the internal power switch. Connect to an external inductor using a wide PCB trace.

THERMAL INFORMATION (continued)

PARAMETER	THERMAL METRIC	QFN-

ELECTRICAL CHARACTERISTICS (continued)

V_{IN}=10V, T_A=-40°C~150°C, typical values are tested under 25°C

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
BUCK2 (LV BUCK)						
V_{IN23}	VIN23 Input Voltage Range		2.7		5	V
V_{OUT2}	VOUT2 Output Voltage			1.8		V
V_{OUT2_ACC}	VOUT2 Accuracy		-2		2	%
$R_{DS\_H\_BK2}$	High-side MOSFET on-resistance	V_{OUT1}=3.1V		155	260	m
$R_{DS\_L\_BK2}$	Low-side MOSFET on-resistance	VIN>5V		75	125	m
$I_{ILEAK\_HS\_BUCK2}$	SW2 HS Switch Leakage Current	T_A=25°C		0.01	1	A
		T_A=-40°C~150°C		7		A
$I_{ILEAK\_LS\_BUCK2}$	SW2 LS Switch Leakage Current			0.01	1	A
I_{PEAK_BUCK2}	Peak Current Limit		0.9	1.2	1.65	A
I_{VALLEY_BUCK2}	Valley Current Limit		0.65	1	1.3	A
$I_{REVERSE\_BUCK2}$	Reverse Current Limit		0.4	0.7	1	A
I_{ILEAK_VOUT2}	VOUT2 PIN Leakage			1	10	A
R_{DIS_BUCK2}	VOUT2 Output Discharge resistance		30	50	70	Ohm
BUCK3 (LV BUCK)						
V_{IN23}	VIN23 Input Voltage Range		2.7		5	V
V_{OUT3}	VOUT3 Output Voltage			1.1/ 1.2/ 1.3/ 1.5		V
V_{OUT3_ACC}	VOUT3 Accuracy		-2		2	%
$R_{DS\_H\_BK3}$	High-side MOSFET on-resistance	V_{OUT1}=3.1V		155	260	m
$R_{DS\_L\_BK3}$	Low-side MOSFET on-resistance	VIN>5V		75	125	m
$I_{ILEAK\_HS\_BUCK3}$	SW3 HS Switch Leakage Current	T_A=25°C		0.01	1	A
		T_A=-40°C~150°C		7		A
$I_{ILEAK\_LS\_BUCK3}$	SW3 LS Switch Leakage Current			0.01	1	A
I_{PEAK_BUCK3}	Peak Current Limit		1.45	2	2.75	A
I_{VALLEY_BUCK3}	Valley Current Limit		1.15	1.7	2.15	A
$I_{REVERSE\_BUCK3}$	Reverse Current Limit		0.4	0.7	1	A
I_{ILEAK_VOUT3}	VOUT3 PIN Leakage			1	10	A
R_{DIS_BUCK3}	VOUT3 Output Discharge resistance		30	50	70	Ohm
LDO						
V_{LDOIN}	LDOIN Input Voltage Range		2.7		5	V
V_{LDO}	LDO Output Voltage			2.7/ 2.8/ 2.9/ 3.3		V
V_{LDO_ACC}	LDO Output Voltage Accuracy		-2		2	%

ELECTRICAL CHARACTERISTICS (continued)

V_{IN}=10V, T_A=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{DROP_LDO}	LDO Dropout Voltage	LDOIN=2.9V, setting LDO output =2.8V, ILDO = 300mA		110	200	mV
$L_{DO\_LINE\_REG}$	LDO Line Regulation	LDOOUT set to 2.7V, LDOIN=3V to 5V, ILDO = 100mA		0.02		%/V
$L_{DO\_LOAD\_REG}$	LDO Load Regulation	LDOIN=3.3V, LDOOUT=2.7V, ILDO from 10mA to 300mA.		0.03		%
I_{LIM_LDO}	LDO Current Limit	LDOIN=3 V, setting LDOOUT to 2.8V, force LDOOUT=2.5V	350	400	460	mA
$PSRR_{\_LDO}$(1)	LDO PSRR	LDOIN= 3.1V, LDOOUT=2.8V, C(NR)=100nF, COUT=20 F, ILDO = 100mA @ 1kHz		70		dB
		LDOIN= 3.1V, LDOOUT=2.8V, C(NR)=100nF, COUT=20 F, ILDO = 100mA @ 10kHz		56		dB
		LDOIN= 3.1V, LDOOUT=2.8V, C(NR)=100nF, COUT=20 F, ILDO = 100mA @ 100kHz		35		dB
		LDOIN= 3.1V, LDOOUT=2.8V, C(NR)=100nF, COUT=20 F, ILDO = 100mA @ 1MHz		29		dB
		LDOIN= 3.1V, LDOOUT=2.8V, C(NR)=100nF, COUT=20 F, ILDO = 100mA @ 2.2MHz		24		dB
$eN_{\_LDO}$(1)	LDO noise	LDOIN= 3.1V, LDOOUT=2.8V, C(NR)=100nF, COUT=20 F, ILDO = 100mA, From 10Hz to 100kHz		30		V_{rms}
I_{ILEAK_LDOOUT}	LDOOUT(VOUT4) PIN Leakage			0.01	1	A
R_{DIS_LDO}	LDOOUT(VOUT4) Output Discharge resistance		30	50	70	Ohm
Power Good OV/UV threshold						
PGOV	Vout1/2/3/4 Power Good Over Voltage Threshold, Rising		105	110	115	%
	Hysteresis			2.5		%
PGUV	Vout1/2/3/4 Power Good Under Voltage Threshold, Falling		85	90	95	%
	Hysteresis			2.5		%
Protection						
$V_{OUT,OVP}$	Vout1/2/3/4 Over Voltage Threshold, Rising		115	120	125	%
	Hysteresis			5		%
$V_{OUT,UVP}$	Vout1/2/3/4 Under Voltage Threshold, Falling		70	75	80	%
	Hysteresis			5		%
$V_{IN,OVP}$	VIN Over Voltage Threshold, Rising		19.5	21	22.5	V
	Hysteresis			1		V
T_{SD}						

TYPICAL CHARACTERISTICS

V_{IN}=10V, T_A=-40°C~125°C, unless otherwise noted.

Figure 1. Buck1 Efficiency vs Load Current, V_{OUT1}=3.2V

Figure 2. Buck1 Efficiency vs Load Current, V_{OUT1}=3.0V

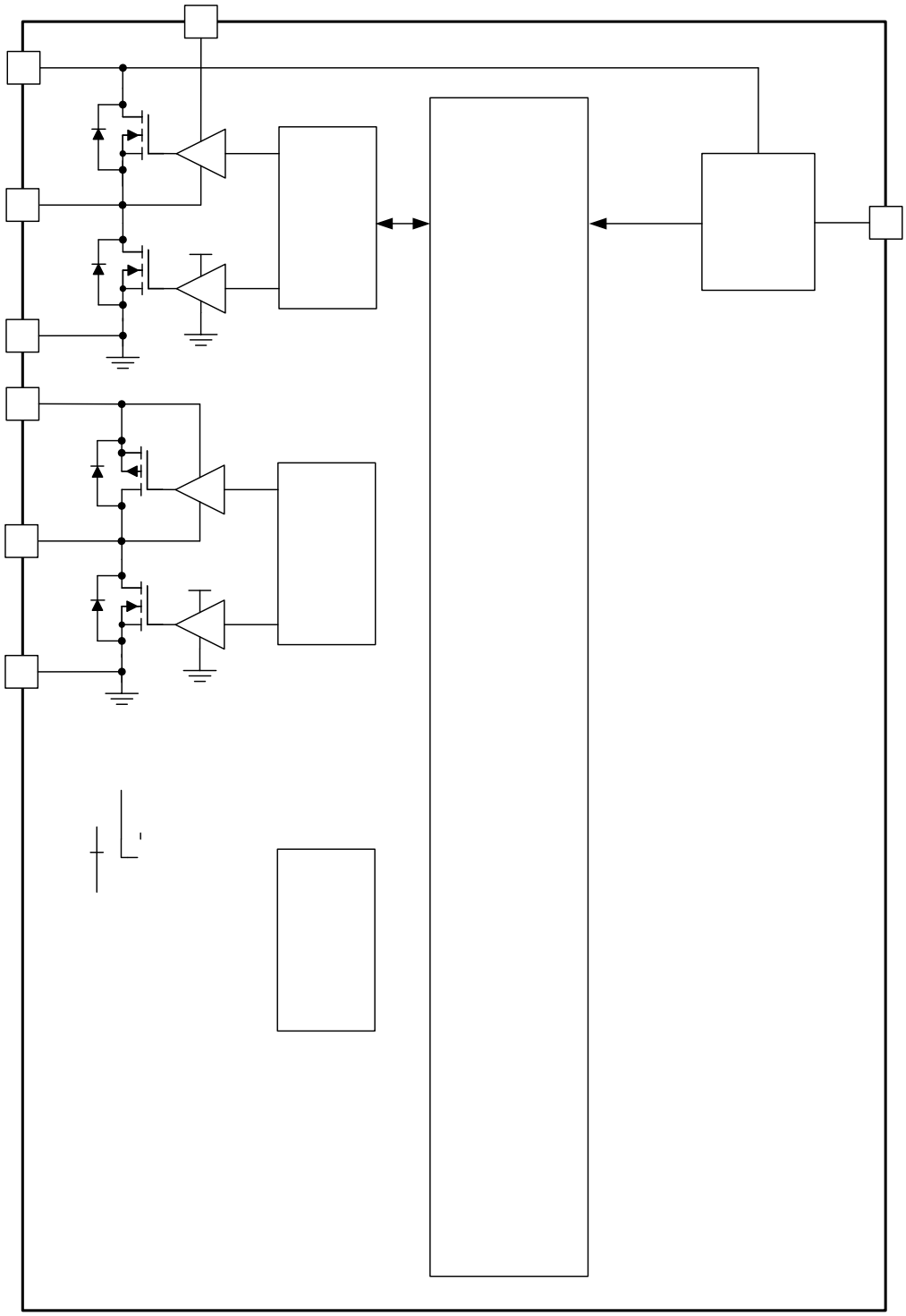
Figure 3. Buck2 Efficiency vs. Load Current, V_{OUT2}=1.8V

Figure 4. Buck3 Efficiency vs. Load Current, V_{OUT3}=1.2V

Figure 5. Buck3 Efficiency vs. Load Current, V_{OUT3}=1.5V

Figure 6. Buck1 Peak Current Limit vs. Temperature

FUNCTIONAL BLOCK DIAGRAM



OPERATION

Overview

The SCT61240Q is a highly integrated power management IC (PMIC) optimized for automotive camera system. It integrates three high efficiency synchronous BUCK converters (HVBUCK1, LVBUCK2, LVBUCK3), and a high-PSRR low noise LDO with OV/UV monitoring on all outputs.

VOUT1 is the output of BUCK1, which is powered from VIN (Power Over Coax) and can output 1.2A continuous current with the output voltage set to LDOOUT+300mV/500mV or fixed 3.3V.

VOUT2 is the output of BUCK2, which is powered from VOUT1 and can output 600mA continuous current with the output voltage fixed to 1.8V.

VOUT3 is the output of BUCK3, which is powered from VOUT1 and can output 1.2A continuous current with the output voltage set to 1.1V/1.2V/1.3V/1.5V through RSET PIN for different sensors.

LDOOUT is the output of LDO, which is powered from VOUT1 (need to connect LDOIN to VOUT1) and can output 300mA continuous current with the output voltage set to 2.7V/2.8V/2.9V/3.3V through RSET PIN for different sensors.

With a compact QFN2.5x3.5 package, the SCT61240Q greatly reduces external components count and PCB space.

VIN and EN UVLO

When the VIN pin voltage rises above 3.8V and the EN pin voltage exceeds the enable threshold of 1.2V, the device is enabled. And the device disables when the VIN pin voltage falls below 3.8V or when the EN pin voltage is below 1.1V.

An internal 10M r pulls EN pin to an internal 5V power supply allows the device to be enabled when EN pin is floating to simplify the system design.

High Efficiency Buck Converters

Under Voltage Protection

If an output falls below the under voltage protection threshold, all outputs will shut off for the hiccup time. When hiccup ends, the normal power up sequence will start again according to the SEQ and RSET setting. When entry hiccup, the output discharge will operate during the hiccup time.

Over Current Protection (OCP)

For the three bucks and LDO, the SCT61240Q provides both peak and valley current limit designed to limit the peak/valley inductor current to ensure that the switching currents remain within the device capabilities during overload conditions or during an output short circuit.

When the HS-FET turns on, the chip monitors the increased IL through the relevant operating main power switch. Once the peak IL exceeds the peak current limit threshold, the HS-FET turns off immediately, and the LS-FET turns on to conduct and decrease IL. The HS-FET does not turn on again until IL falls below the valley current limit threshold.

Power Good

The PG pin is a push-pull output. It goes to logic high when the device is powered on, and all outputs are within the power good range, and no faults reported. The high output level can be programmed to either 3.3V or 1.8V.

PG will assert low when any of below events occur:

- Buck1's output is out of power good range or VOUT OV/UV range
- Buck2's output is out of power good range or VOUT OV/UV range
- Buck3's output is out of power good range or VOUT OV/UV range
- LDO's output is out of power good range or VOUT OV/UV range
- Junction temperature is over Thermal Shutdown point
- VIN is higher than VIN OVP threshold

Hiccup or Latch off Protection

When below faults are detected, the SCT61240Q will enter hiccup or latch off mode (programmable option). When select hiccup mode and entry hiccup, all the channels shut off for 3.6ms, and then the normal power up sequence will start again according to the SEQ and RSET setting. When select latch off mode and entry latch off, all the channels shut off and not restart unless VIN/EN power on reset (POR).

The faults that make the device entry hiccup/latch off protection:

- Buck1's output is out of VOUT OV/UV range
- Buck2's output is out of VOUT OV/UV range
- Buck3's output is out of VOUT OV/UV range
- LDO's output is out of VOUT OV/UV range
- Junction temperature is over Thermal Shutdown point
- VIN is higher than VIN OVP threshold

Output Discharge

In order to discharge the energy of output capacitor during power off sequence, all channels have active discharge path from their output to ground. The discharge path is turn-on when channel is disabled.

Internal Soft-Start

The soft start function is implemented to prevent the PMIC output voltage from overshooting during start-up. When the PMIC starts up, the internal circuitry of each power rail generates a soft-start voltage that ramps up from 0V. The soft-start period lasts until the voltage on the soft-start capacitor exceeds the reference voltage. At this point, the reference voltage takes over.

Output Voltage Setting

The device provides 9 flexible voltage setting thr 1 >.( )15.3 274 Tc 0ett w60.6 Tm ( )Tj3.m 0.19Tj E (60.E0 Tw767.01 q

APPLICATION INFORMATION

Typical Application

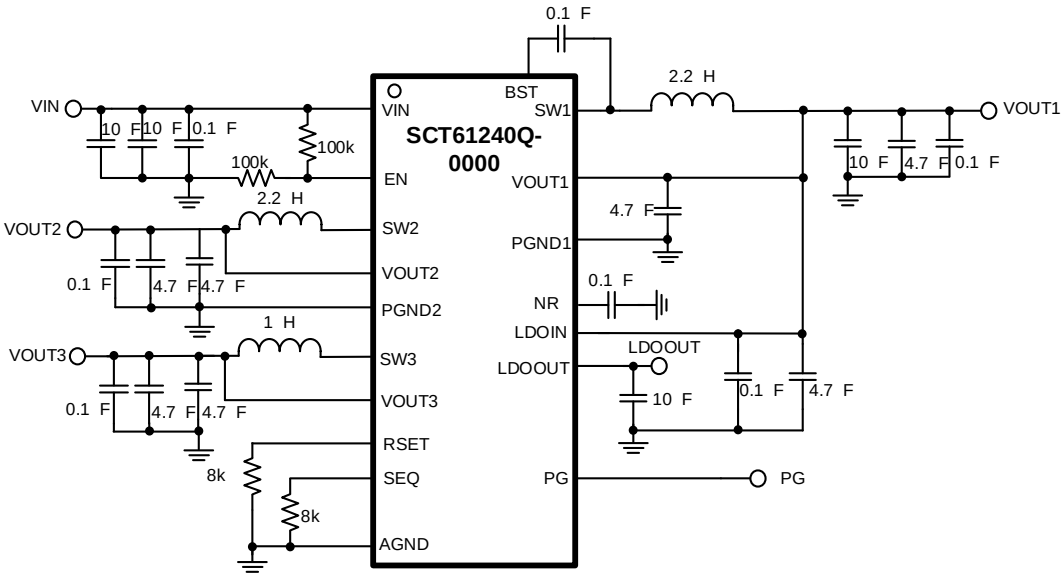


Figure 13. Application Schematic, 4V to 19V, PMIC Regulator at 2.2MHz

Design Parameters

Design Parameters	Example Value
Input Voltage	10V Normal 4V to 19V
Output Voltage	VOUT1: 3.0V VOUT2: 1.8V VOUT3: 1.2V LDOOUT: 2.7V
Maximum Output Current	VOUT1: 1.2A (in total) VOUT2: 0.6A VOUT3: 1.2A LDOOUT: 0.3A
Switching Frequency	2.2MHz
Output Voltage Ripple (peak to peak)	VOUT1: 10mV VOUT2: 2mV VOUT3: 4mV

Under Voltage Lock-Out

An external voltage divider network of R_1 from the input to EN pin and R_2 from EN pin to the ground can set a higher input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. Use Equation 1 and Equation 2 to calculate the values of R_1 and R_2 resistors.

$$= 1 + \frac{1}{2} \quad (1)$$

$$= 1 + \frac{1}{2} \quad (2)$$

where

- V_{rise} is rising threshold of Vin UVLO
- V_{fall} is falling threshold of Vin UVLO
- V_{ENrise} is rising threshold of EN UVLO
- V_{ENfall} is falling threshold of EN UVLO

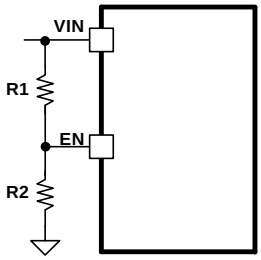


Figure 14. System UVLO by enable divide

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance(DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20%~40% of the maximum output current.

The peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 3.

- $V_{IN(max)}$ is the maximum input voltage
- $I_{OUT(max)}$ is the maximum DC load current
- LIR is coefficient of I_{LPP} to I_{OUT}

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in equation 5 and equation 6.

$$= \quad + \frac{}{2} \tag{5}$$

$$= \sqrt{(\quad)^2 + \frac{1}{12}\ (\quad)^2} \tag{6}$$

Where

- I_{LPEAK} is the inductor peak current
- I_{OUT} is the DC load current
- I_{LPP} is the inductor peak-to-peak current
- I_{LRMS} is the inductor RMS current

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device. The most conservative approach is to choose an inductor with a saturation current rating greater than peak current limit. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the SCT61240Q can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a lower maximum output current.

Input Capacitor Selection

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \quad C_{IN}} \quad \frac{V_{OUT}}{V_{IN}} \quad (1 - \frac{V_{OUT}}{V_{IN}}) \tag{9}$$

For this example, two 10 50 -
frequency filtering capacitor is placed as close as possible to the device pins.

Bootstrap Capacitor Selection

connected between BOOT pin and SW pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 10 desired.

$$\Delta V_{OUT} = \frac{(\quad - \quad)}{8 \quad ^2} \tag{10}$$

Where

- $_{OUT}$ is the output voltage ripple
- f_{SW} is the switching frequency
- L is the inductance of inductor
- C_{OUT} is the output capacitance
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, two 4.
The LDO is specifically designed to work with a standard ceramic output capacitor to save space and improve performance. Larger output capacitors will improve load transient response and reduce noise at the cost of 20 stable output.

Application Waveforms

Vin=10V, RSET=SEQ=8kΩ, V_{OUT1}=3.0V, V_{OUT2}=1.8V, V_{OUT3}=1.2V, V_{OUT4}=2.7V,unless otherwise noted

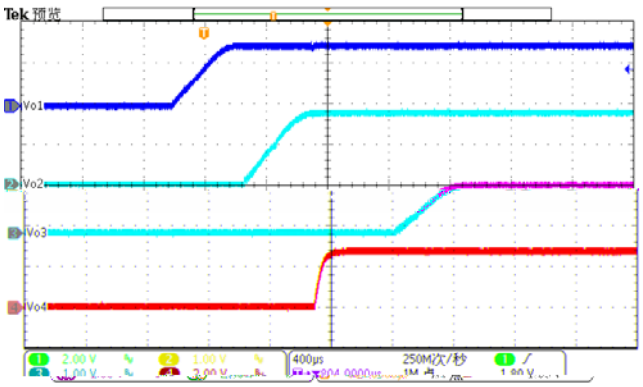


Figure 15. Power On (Io2=0.6A, Io3=1.2A, Io4=0.3A)

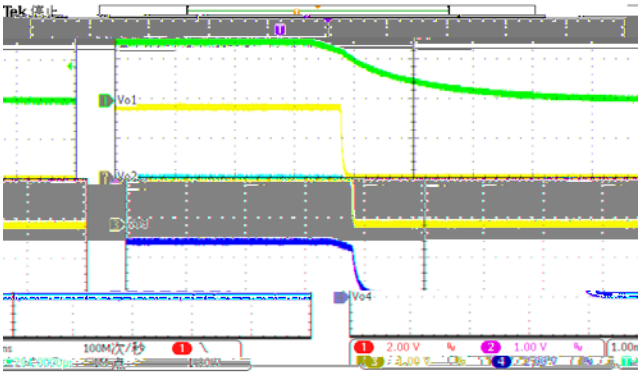


Figure 16. Power Off (Io2=0.6A, Io3=1.2A, Io4=0.3A)

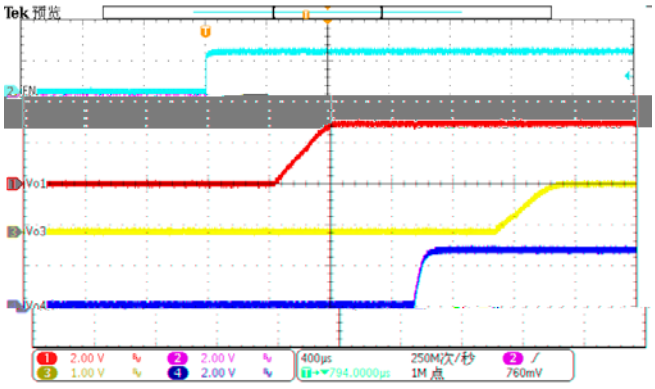


Figure 17. EN On (Io2=0.6A, Io3=1.2A, Io4=0.3A)

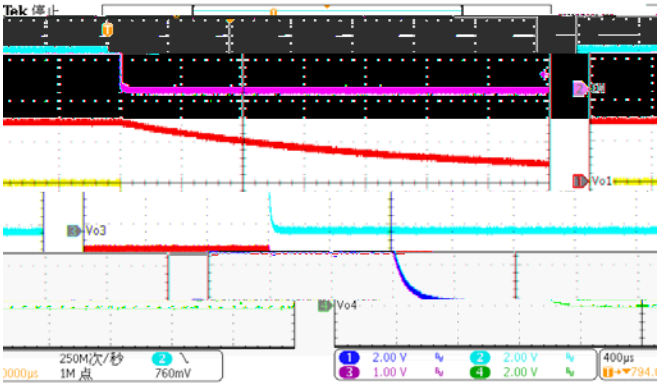


Figure 18. EN Off (Io2=0.6A, Io3=1.2A, Io4=0.3A)

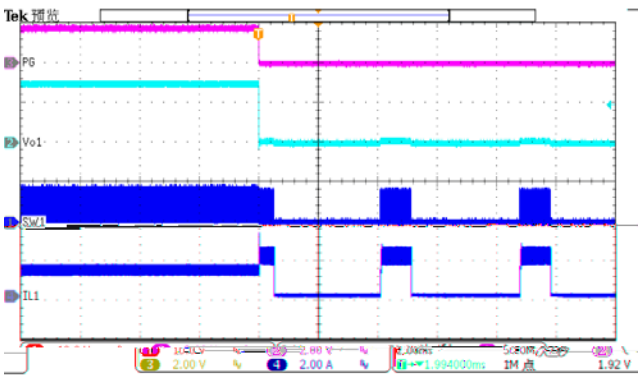


Figure 19. Buck1 Over Current Protection
(1.2A to hard short)

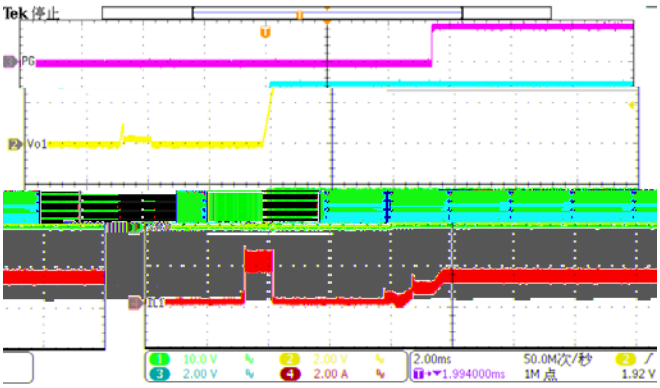


Figure 20. Buck1 Over Current Release
(hard short to 1.2A)

Application Waveforms (continued)

Vin=10V, RSET=SEQ=8kΩ, V_{OUT1}=3.0V, V_{OUT2}=1.8V, V_{OUT3}=1.2V, V_{OUT4}=2.7V,unless otherwise noted

Figure 21. Buck2 Over Current Protection

(0.6A to hard short)

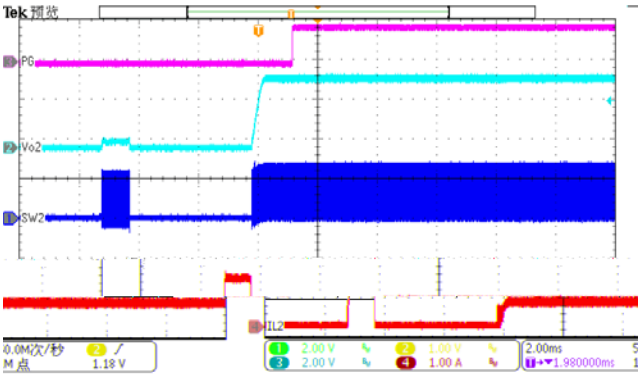


Figure 22. Buck2 Over Current Release

(hard short to 0.6A)

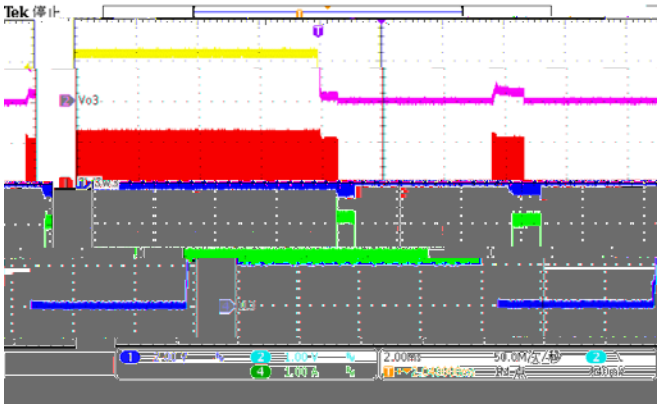


Figure 23. Buck3 Over Current Protection

(1.2A to hard short)

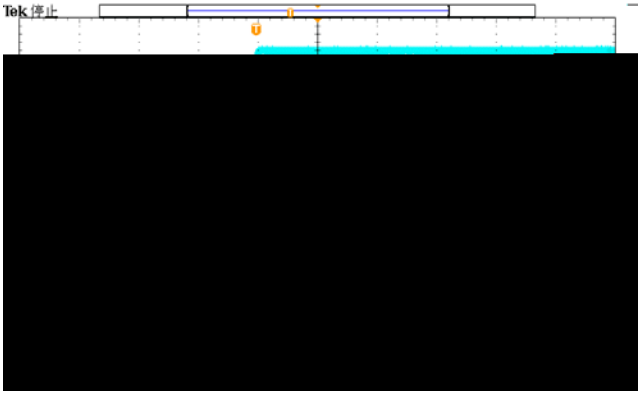


Figure 24. Buck3 Over Current Release

(hard short to 1.2A)

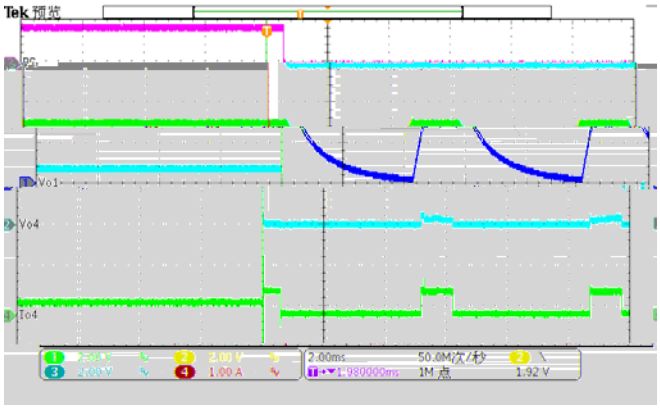


Figure 25. LDO Over Current Protection

(0.3A to hard short)

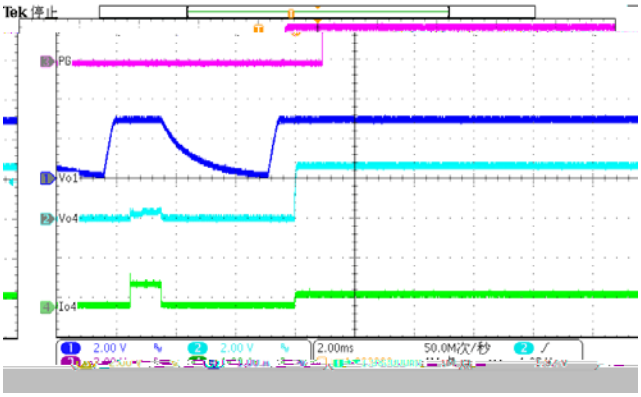


Figure 26. LDO Over Current Release

(hard short to 0.3A)

Application Waveforms (continued)

Vin=10V, RSET=SEQ=8kΩ, V_{OUT1}=3.0V, V_{OUT2}=1.8V, V_{OUT3}=1.2V, V_{OUT4}=2.7V,unless otherwise noted

Figure 27. Buck1 Steady State (Io1 = 1.2A)

Figure 28.

Layout Guideline

Proper PCB layout is a critical for SCT61240Q's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.

2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.

3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.

4. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias.

5. Output inductor should be placed close to the SW pin. The switching area of the PCB conductor minimized to prevent excessive capacitive coupling.

6. UVLO adjust resistors and feedback trace should connect to small signal ground which must return to the GND pin without any interleaving with power ground.

7. For LDO low noise area, place an independent copper plane with AGND pin. Use this quiet AGND through LDO power path and sensitive pins NR, RSET, SEQ. To avoid noise interference, using vias to connect AGND to PGND with single point.

8. For achieving better thermal performance, a four-layer layout is strongly recommended.

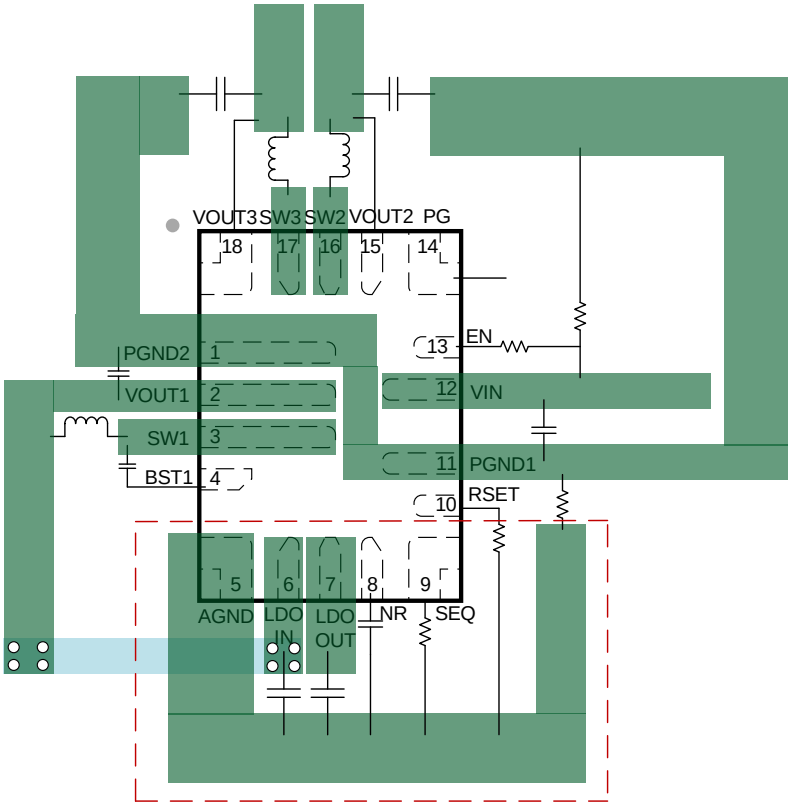
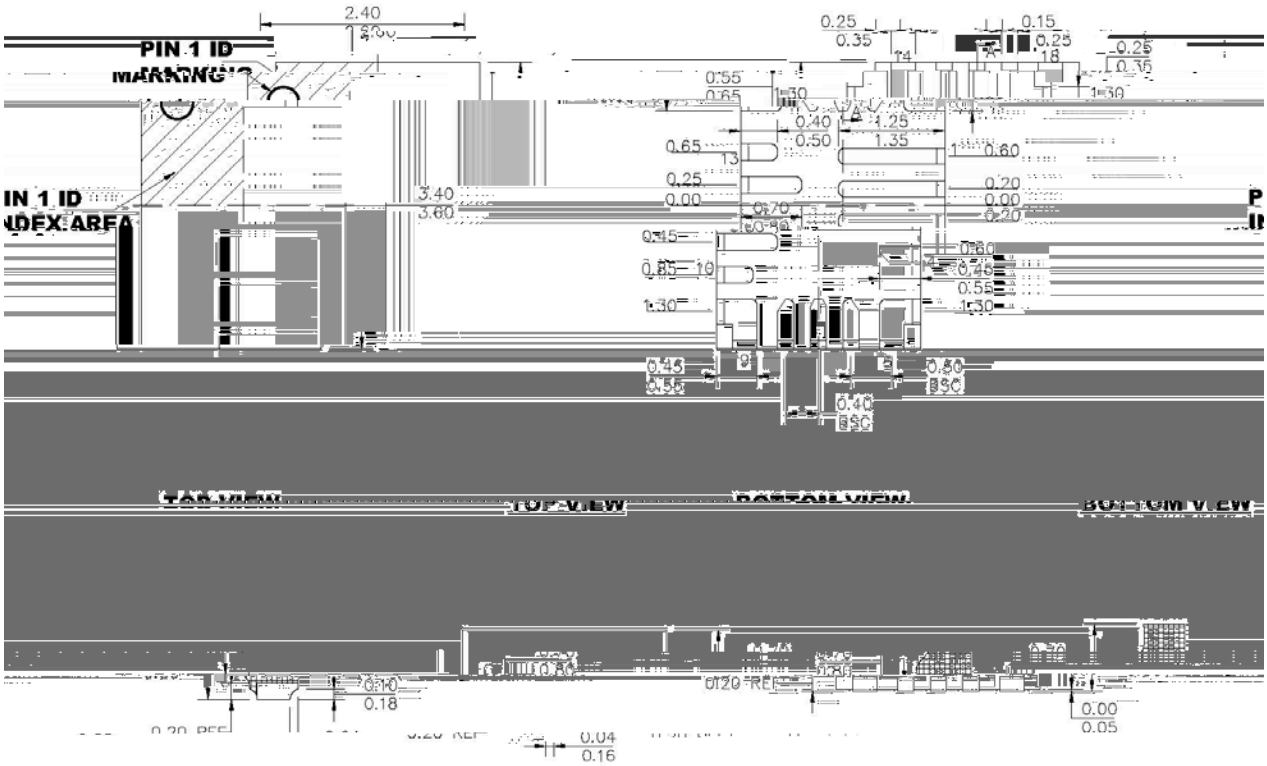
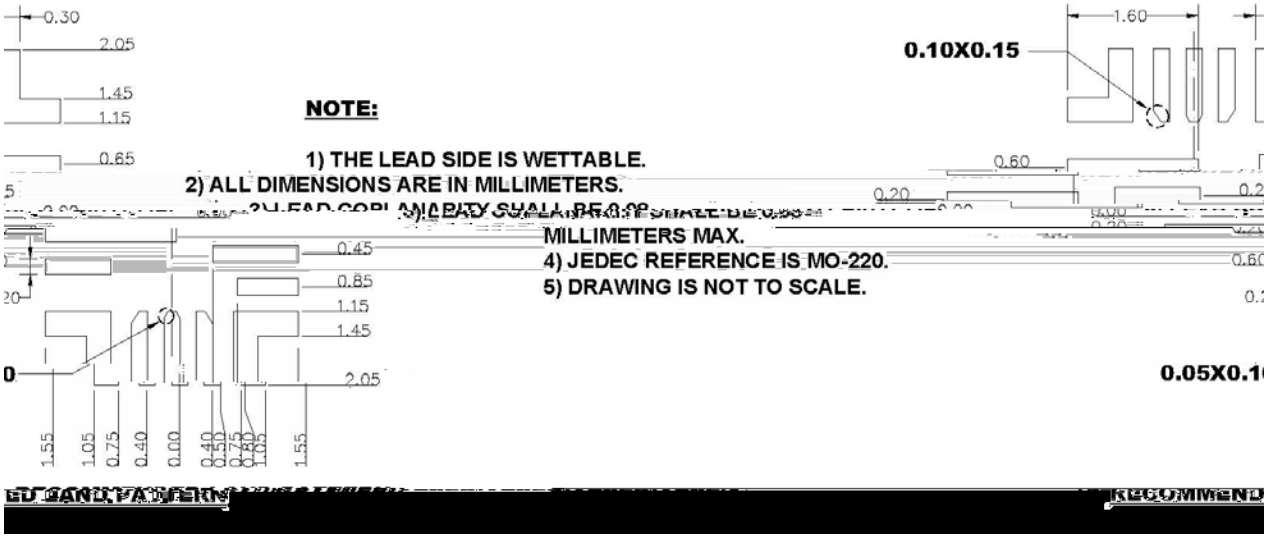


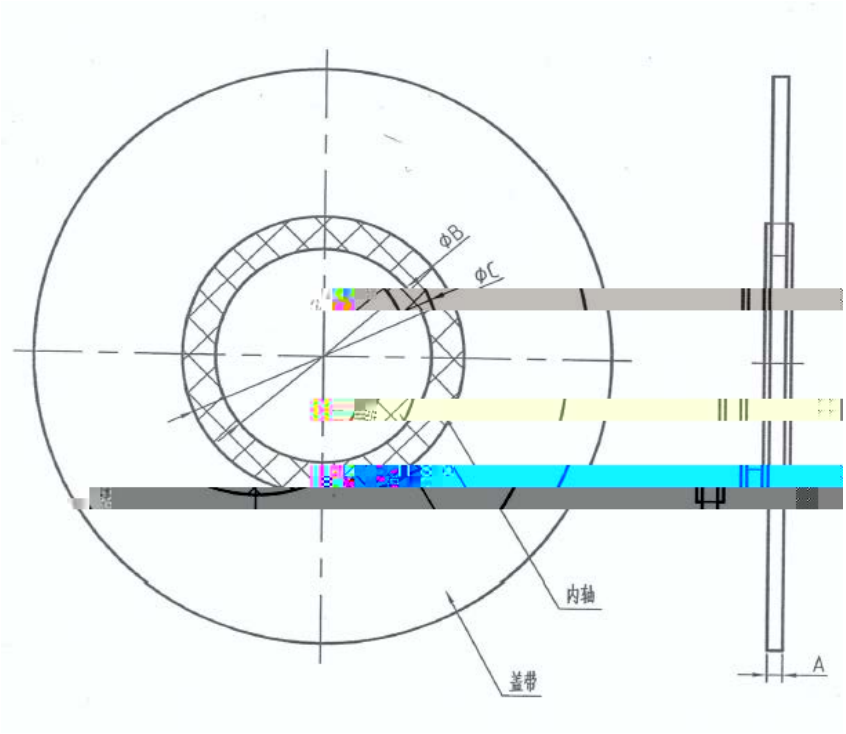
Figure 31. PCB Layout Example

PACKAGE INFORMATION

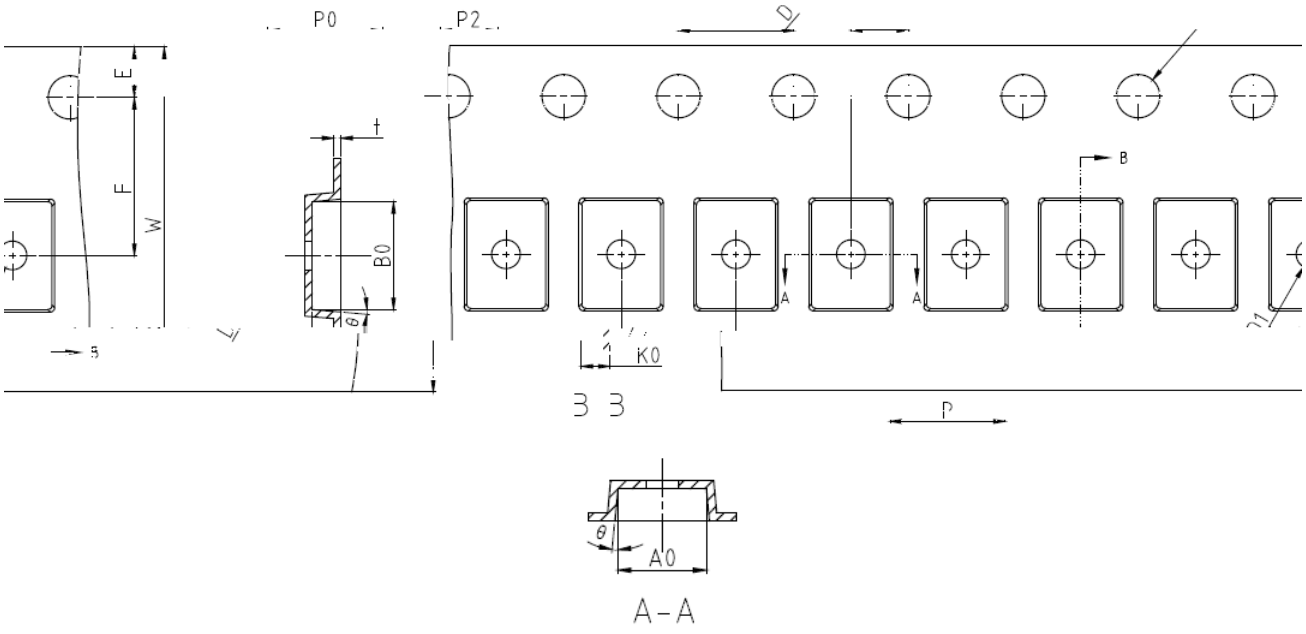




TAPE AND REEL INFORMATION



Type	$A_0^{+0.1}$ mm	Carrier Width	Diameter
PRA F4DK	9.3	12	B=76.2±0.10mm C=92.2±0.25mm
HST	9.5	12	
HST	13.5	16	
HST C800	21.3	24	
2420S	13.3	16	
2420S	21.3	24	
TIST300	9.9	12	



Symbol	Dimensions in Millimeters
A0	2.75±0.10
B0	3.75±0.10
D	$1.5^{+0.10}$
D1	1.00±0.10
E	1.75±0.10
F	5.50±0.05
K0	1.00±0.10
P	4.00±0.10
P0	4.00±0.10
P2	2.00±0.05
t	0.25±0.03
W	$12.00^{+0.30}_{-0.10}$
	5 ° max

