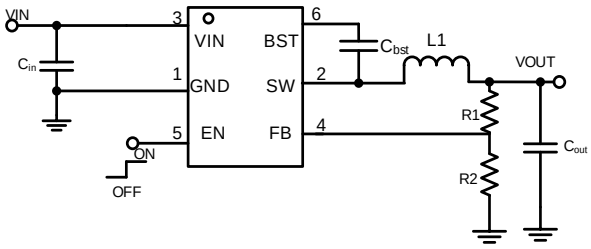
L LL d I d hede I e d ed h h

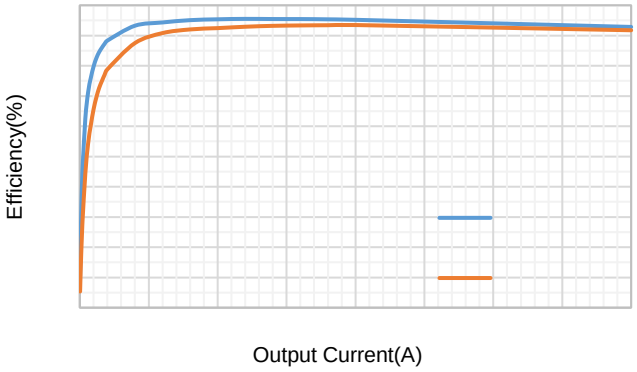
C H ed

KH I I H F ED

FF EDI

OF FF ED





H L I ED I EHO

L EH H D EHC ED

IE K C N CKC H D I

Over operating free-air temperature unless otherwise noted (1)

DESCRIPTION	MIN	MAX	UNIT
BST	-0.3	38	V
VIN (2)	-0.3	32	V
SW	-0.3	32	V
SW (<10ns) (3)	-3	32	V
BST-SW	-0.3	5.5	V
EN, FB	-0.3	5.5	V
Operating junction temperature (4)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

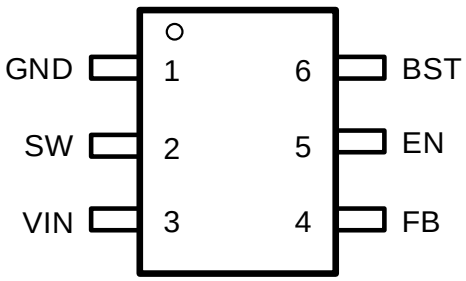
(1)

(2)

(3)

(4)

F D ED KH ED



Top View: SOT23-6L, Plastic

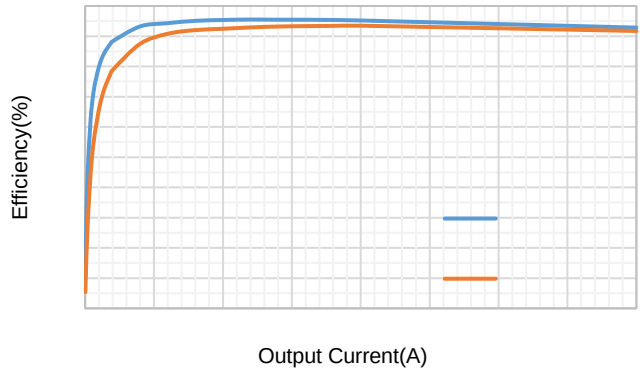
D E qa$S—q$yñ Ò(b4 Uf“&Âë I Á P¤)T7ÂGŸ "†#A•Vi a"ë

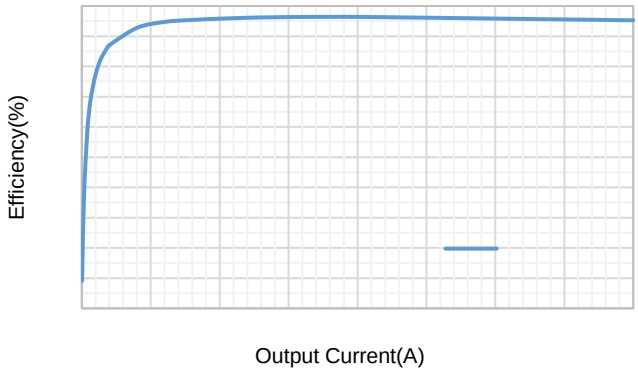
H EC C D EF H D ED EDI

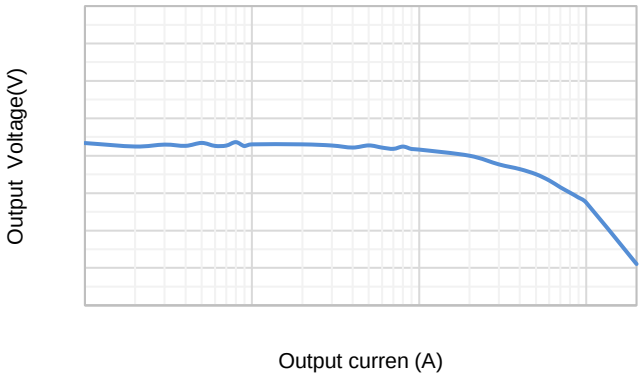
I H D I

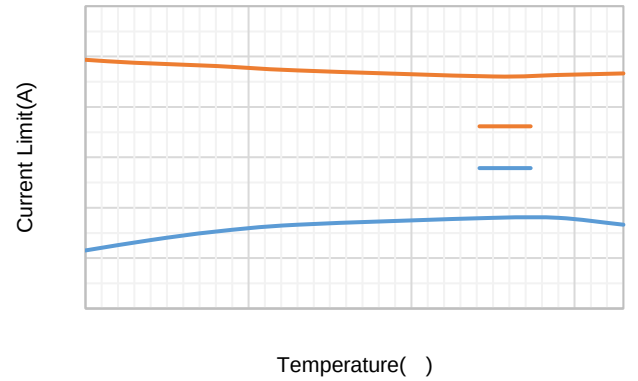
H H H I I

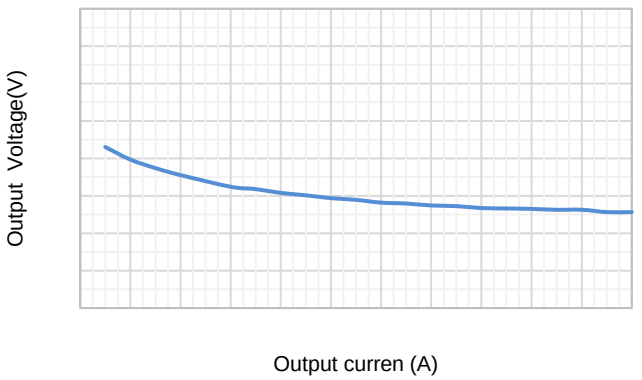
OF H H I I

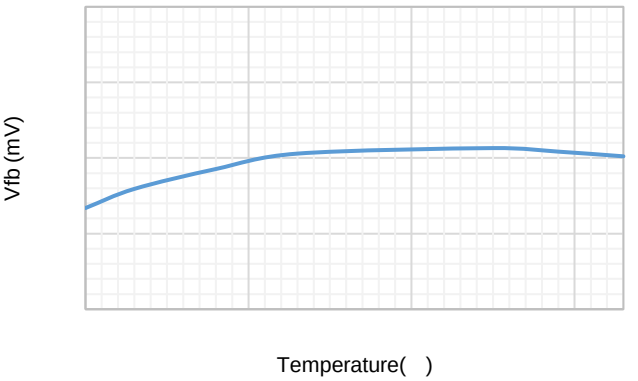

Efficiency(%)
Output Current(A)


Efficiency(%)
Output Current(A)

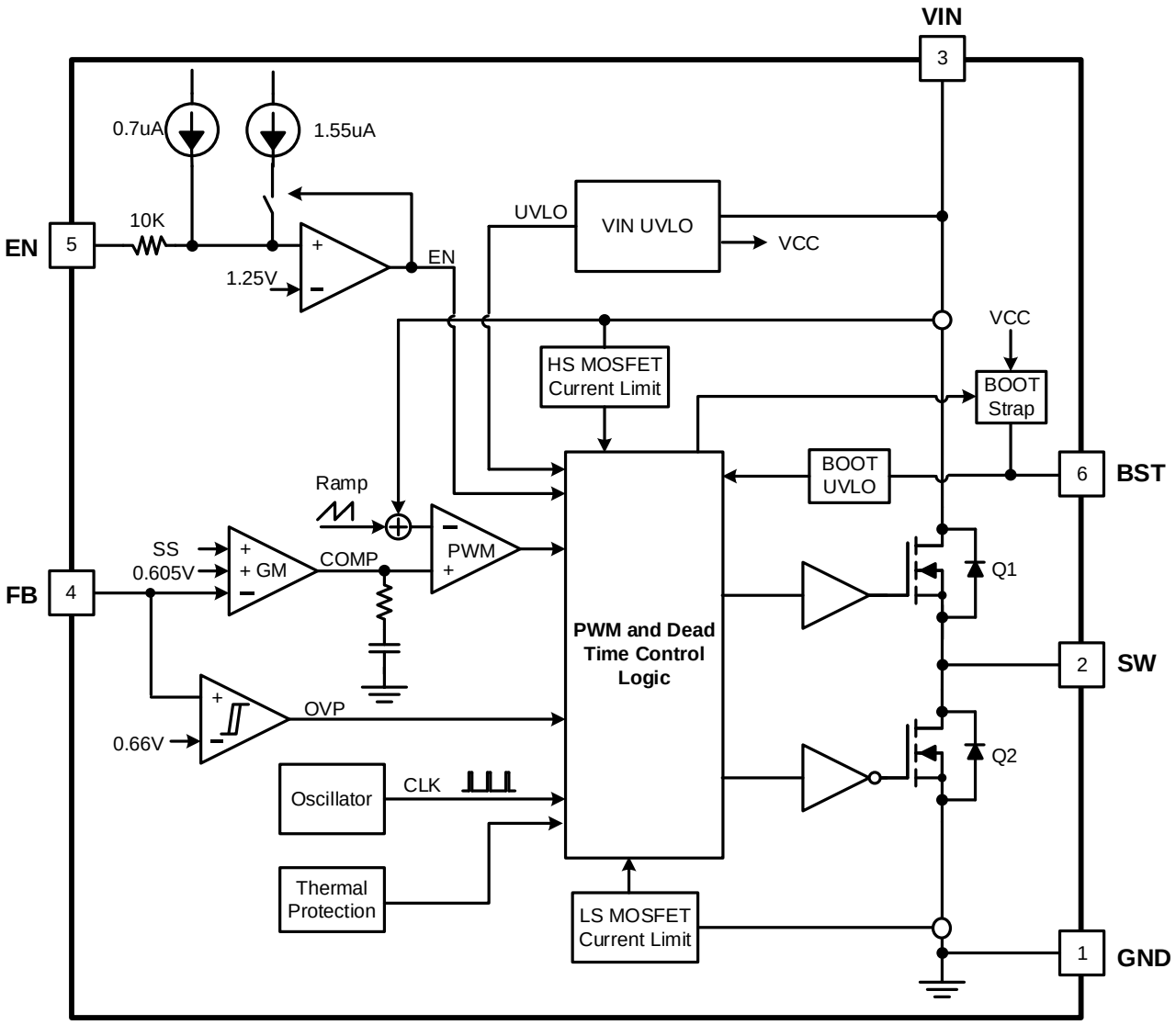

Output Voltage(V)
Output curren (A)


Current Limit(A)
Temperature( )

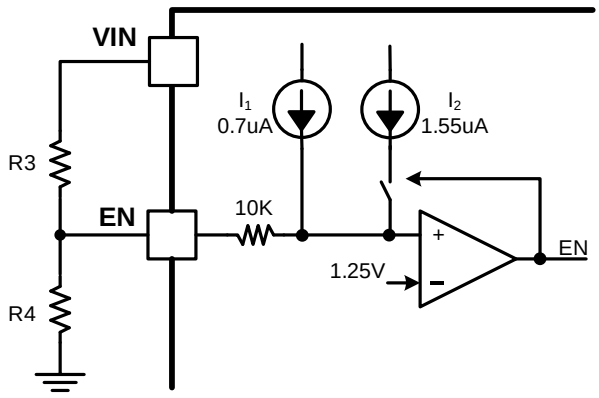

Output Voltage(V)
Output curren (A)


Vfb (mV)
Temperature( )

KD ED E H C


VIN
3
0.7uA
1.55uA
EN
5
10K
1.25V
EN
UVLO
VIN UVLO
VCC
VCC
HS MOSFET
Current Limit
BOOT
Strap
BOOT
UVLO
6
BST
Ramp
SS
0.605V
+ GM
COMP
PWM
FB
4
PWM and Dead
Time Control
Logic
Q1
2
SW
OVP
0.66V
Q2
Oscillator
CLK
Thermal
Protection
LS MOSFET
Current Limit
1
GND

EF H ED

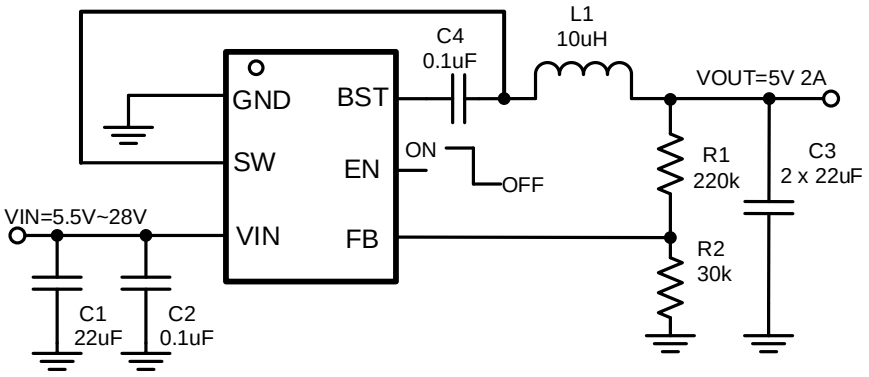


$$S4 \quad \frac{W_T \quad \frac{W_{FO}}{W_{FOS}} \quad W_{T\,p}}{{}_2\,2\,\frac{W_{FO}}{W_{FOS}}\,{}_3} \tag{1}$$

$$S \quad \frac{S_4 \quad W_{FO}}{W_{T\,p} \quad W_{FO} \quad S_4\ {}_2\ {}_3} \tag{2}$$

The inductor current is monitored during high-side MOSFET Q1 and low-side MOSFET Q2 on. The SCT2321E implements over current protection with cycle-by-cycle limiting high-side MOSFET peak current and low-side MOSFET valley current to avoid inductor current running away during unexpected overload or output hard short condition.

FF ED D EHC ED



Design Parameters	Example Value
Input Voltage	12V typical, 5.5~28V
Output Voltage	5V
Output Current	2A
Output voltage ripple (peak to peak)	8mV
Switching Frequency	410kHz

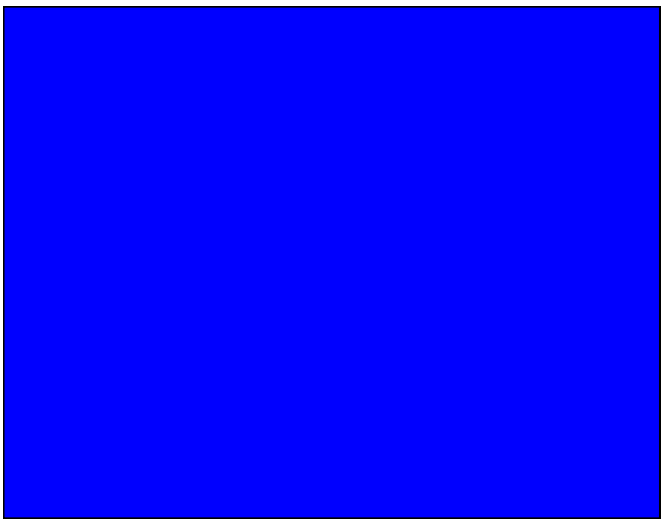
$$W_O \quad \frac{PVU}{D_O \quad TX} \quad \frac{\text{VU}}{\text{O}}$$

VU $\frac{W_{PVU} \quad W_O \quad W_{PVU}}{{}_{TX}{}^{3} \quad M \quad D_{PVU} \quad W_O}$

VU

$$S_2 \quad \frac{W_{PVU} \quad W_f \quad S_3}{W_f} \tag{7}$$

)LJXUH



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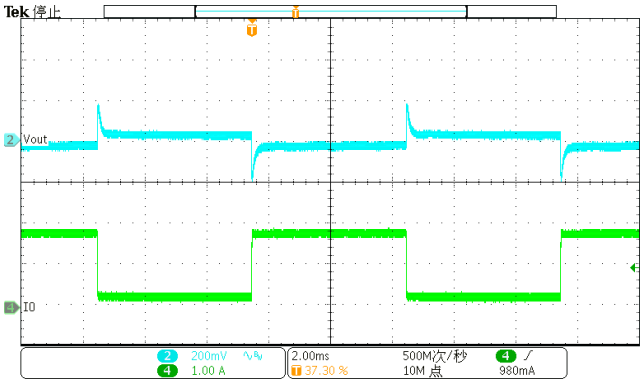
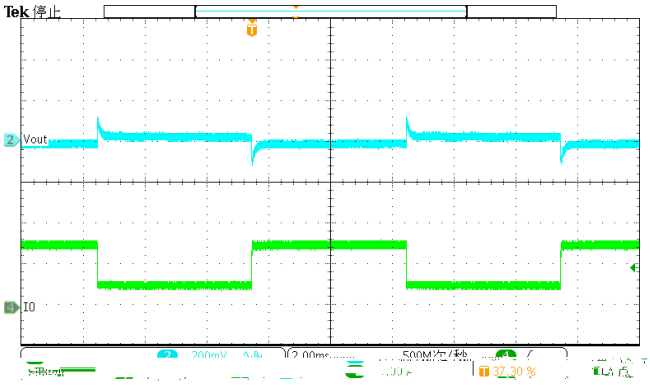
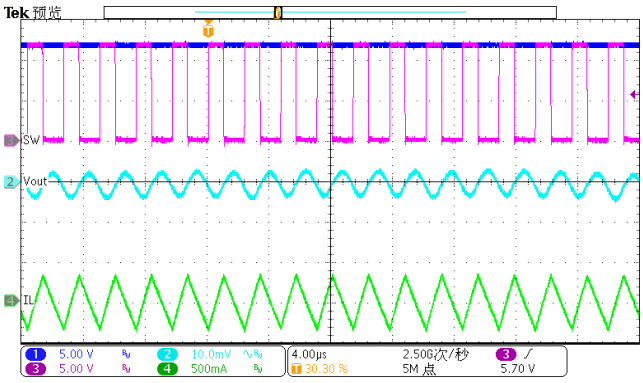
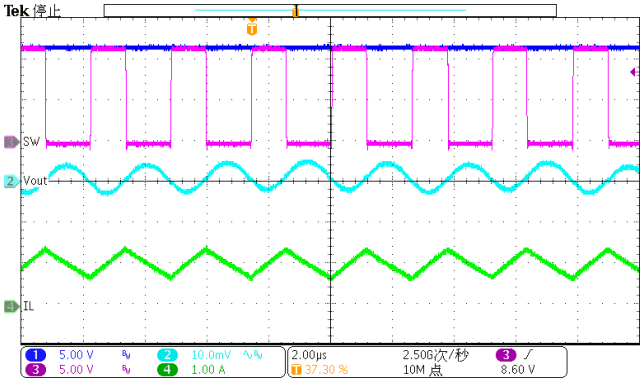
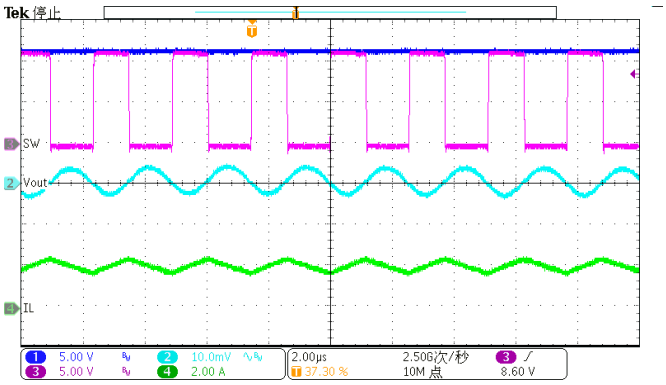

Tek 停止
Vout
IO
200mV
1.00 A
2.00ms
37.30 %
500M次/秒
10M 点
980mA


Tek 停止
Vout
IO


Tek 预览
SW
Vout
IL
5.00 V
5.00 V
10.0mV
500mA
4.00µs
30.30 %
2.50G次/秒
5M 点
5.70 V


Tek 停止
SW
Vout
IL
5.00 V
5.00 V
10.0mV
1.00 A
2.00µs
37.30 %
2.50G次/秒
10M 点
8.60 V


Tek 停止
SW
Vout
IL
5.00 V
5.00 V
10.0mV
2.00 A
2.00µs
37.30 %
2.50G次/秒
10M 点
8.60 V

FLUKE
63.9°C
自动 1
67.5
24.4
ε=0.95
BG=25.0
T=100%
8/1/25
04:36:46 PM

1.

2.

3.

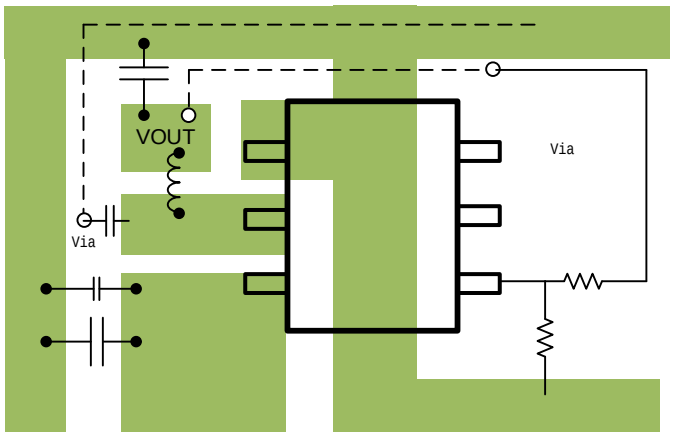
4.

5.

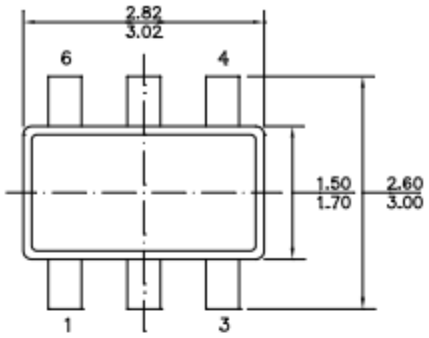
6.

7.

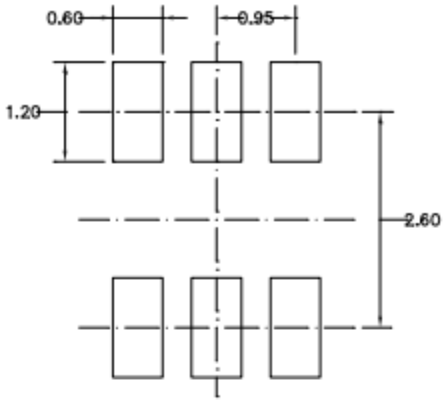
8.



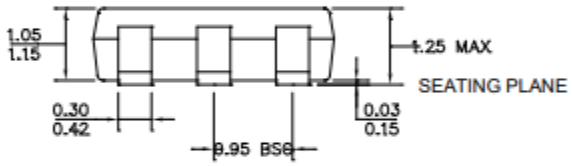
F D EHC ED

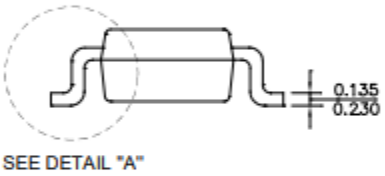


TOP VIEW



RECOMMENDED LAND PATTERN

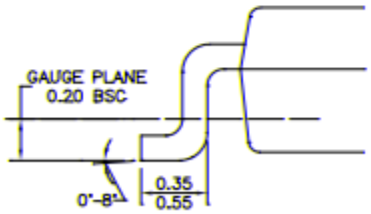




FRONT VIEW **SIDE VIEW**

NOTE:

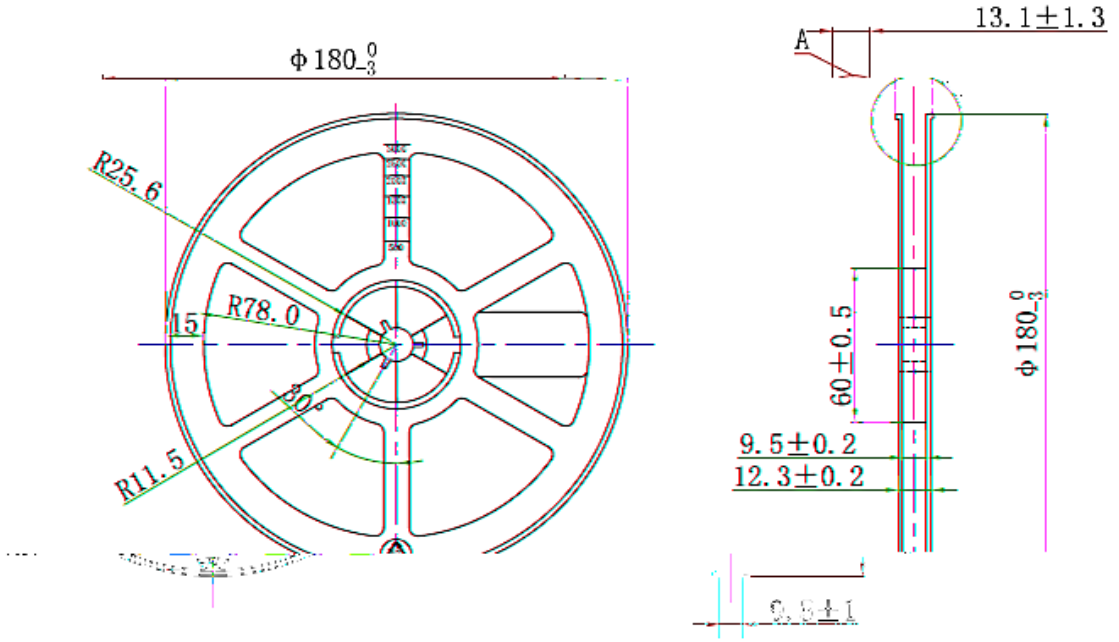
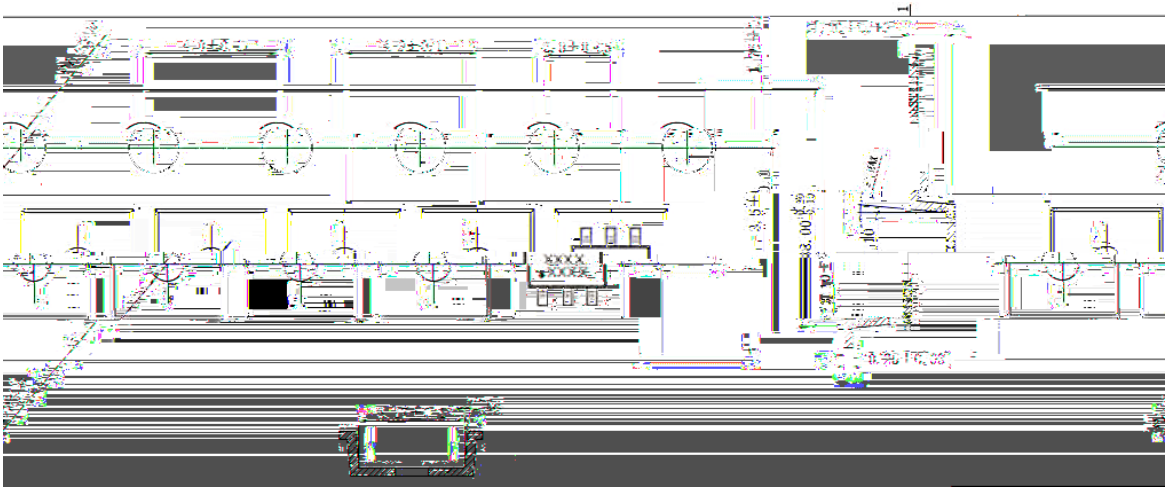
)IMENSIONS ARE IN MILLIMETERS.
(AGE LENGTH DOES NOT INCLUDE MOLD FLASH,
)SION OR GATE BURR.
(AGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH
)TRUSION.
) COPLANARITY (BOTTOM OF LEADS AFTER
)G) SHALL BE 0.10 MILLIMETERS MAX.
)ING CONFORMS TO JEDEC MO-193, VARIATION AB.
)ING IS NOT TO SCALE.
IS LOWER LEFT PIN WHEN READING TOP MARK
(EFT TO RIGHT, (SEE EXAMPLE TOP MARK)



DETAIL "A"

1) ALL D
2) PACK
PROTRU
3) PACK
OR PRO
4) LEAD
FORMIN
5) DRAW
6) DRAW
7) PIN 1
FROM L

F D H D EHC ED


Φ180 0 -3
R25.6
15
R78.0
30°
R11.5
13.1±1.3
A
60±0.5
Φ180 0 -3
9.5±0.2
12.3±0.2
0.5±1