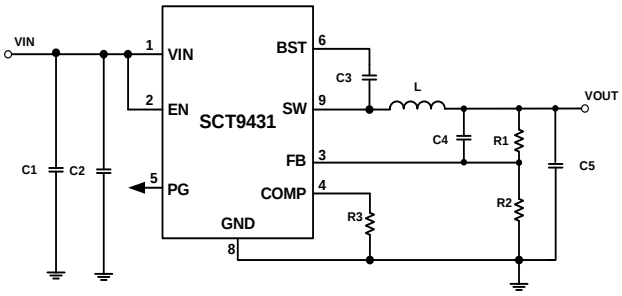
- 3.8V-36V Wide Input Voltage Range
- Up to 3A Continuous Output Load Current
- EMI Reduction
  - Proprietary Gate Design for Switching Node Ringing-free
  - Frequency Spread Spectrum (FSS)
- Pulse Skipping Mode (PSM) with 22uA Quiescent Current in Light Load Condition
  - Up to 79% Efficiency at 1mA Light Load
  - Up to 89% Efficiency at 10mA Light Load
- 0.8V ±1% Feedback Reference Voltage
- Fully Integrated 74mΩ R_{dson} High Side MOSFET and 40mΩ R_{dson} Low Side MOSFET
- 1uA Shut-down Current
- 400kHz Switching Frequency
- Precision Enable Threshold for Programmable UVLO Threshold and Hysteresis
- Output Over Voltage Protection
- Thermal Shutdown Protection at 170°C

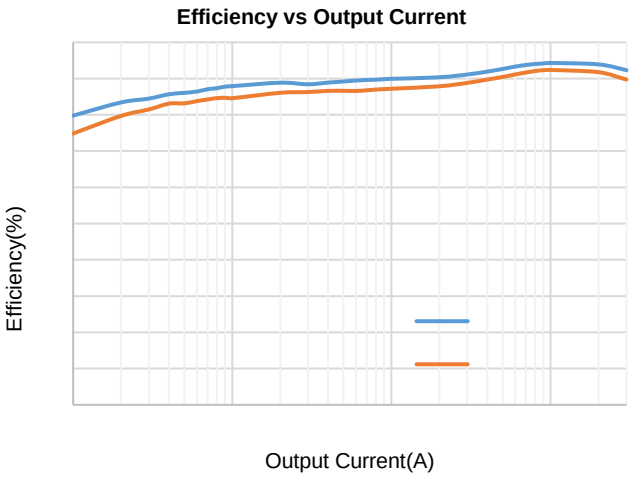
The SCT9431 are 3A synchronous buck converters with up to 36V wide input voltage range, which fully integrates an 74mΩ high-side MOSFET and a 40mΩ low-side MOSFET to provide high efficiency step-down DCDC conversion. The SCT9431 adopts peak current mode control with integrated compensation network. The SCT9431 supports the Pulse Skipping Modulation (PSM) with typical 22uA Ultra-Low Quiescent.

The SCT9431 are optimized for Electromagnetic Interference (EMI) reduction. The converter has proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching. The converter features Frequency Spread Spectrum (FSS) with a switching frequency jitter of ±6%, which reduces EMI by not allowing emitted energy to stay in any one frequency for a significant period of time.

The SCT9431 offer output over-voltage protection, cycle-by-cycle peak current limit, and thermal shutdown protection. The device is available in a low-profile QFN-9L 3mm X 2mm package.

- Automotive System
- Industrial Control System
- General Consumer





Revision 1.0: Production.
Revision 1.1: Update EC table.
Revision 1.2: Update Shutdown current in EC table.
Revision 1.3: Update DEVICE ORDER INFORMATION.
Revision 1.4: Add MSL and description of LDO functionality.

PG	5	Open drain power-good output that is pulled to GND when the output voltage is out of its regulation limits or during soft-start. There is an internal 5MΩ pull-up resistor.
BST	6	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BST pin and SW node.
NC	7	NC
GND	8	Power ground. Must be soldered directly to ground plane.
SW	9	Switching node of the buck converter.

Over operating free-air temperature range unless otherwise noted

. 0 2 0	, 2 - ,	,	6	3, 2
V_{IN}	Input voltage range	3.8	36	V
T_A	Operating Ambient Temperature Range	-40	125	°C
T_J	Operating junction temperature	-40	150	°C

. 0 2 0	, 2 - ,	,	6	3, 2
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(1)	-1	+1	kV

. 0 2 0	2 0 20	/ , !	3, 2
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	61.33	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.24	
Ψ_{JB}	Junction-to-board characterization parameter(1)	5.43	
$R_{\theta JCtop}$	Junction to case(top) thermal resistance(1)	62.99	
$R_{\theta JB}$	Junction-to-board thermal resistance(1)	5.6	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT9431 is mounted. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT9431. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

V_{IN}=12V, T_J=-40°C~150°C, typical value is tested under 25°C.

17 -	. 0 2 0	2 12 -, 2-,	, 27. 6			3, 2
. M CP1 NNJ LB- N						
V_{IN}	Operating input voltage		3.8		36	V
V_{IN_UVLO}	Input UVLO	V_{IN} rising	3.3	3.5	3.7	V
	Hysteresis			420		mV
I_{SD}	Shutdown current	EN=0, No load, VIN=12V		0.6	5	uA
I_Q	Quiescent current	EN=floating, No load, No switching. VIN=12V. BST-SW=5V		22	40	uA
L JC 1MD1 P LB5 MRI GLE MBCQ						
V_{EN_H}	Enable high threshold		1.08	1.18	1.28	V
V_{EN_L}	Enable low threshold		0.98	1.1	1.18	V
I_{EN_L}	Enable pin input current	EN=1V	1	1.5	2	uA
I_{EN_H}	Enable pin input current	EN=1.5V		5.5		uA
. M CP - 1 2Q						
R_{DSON_H}	High side FET on-resistance			74	130	mΩ
R_{DSON_L}	Low side FET on-resistance			40	70	mΩ
CCB AI LB PRMP KNJGGP						
V_{FB}	Feedback Voltage	T_J =25	0.792	0.8	0.808	V
		T_J =-40 -150	0.788	0.8	0.812	V
PRCL CK G						
I_{LIM_HSD}	HSD peak current limit	T_J =25	4.0	4.5	5.0	A
		T_J =-40 -150	3.7	4.5	5.3	
I_{LIM_LSD}	LSD valley current limit			4		A
1 GAFGLE PCO CLA						
F_{SW}	Switching frequency	V_{IN}=12V, V_{OUT}=5V, T_J =25	350	400	450	kHz
		V_{IN}=12V, V_{OUT}=5V, T_J =-40 -150	330		470	kHz
t_{ON_MIN}	Minimum on-time			100		ns
1MD1 P 2CK C						
t_{SS}	Internal soft-start time			4		ms
. RM CA GML						
V_{OVP}	Output OVP threshold	V_{OUT} rising Hysteresis		110 5		% %
T_{SD}	Thermal shutdown threshold*	T_J rising Hysteresis		170 25		°C

*Derived from bench characterization

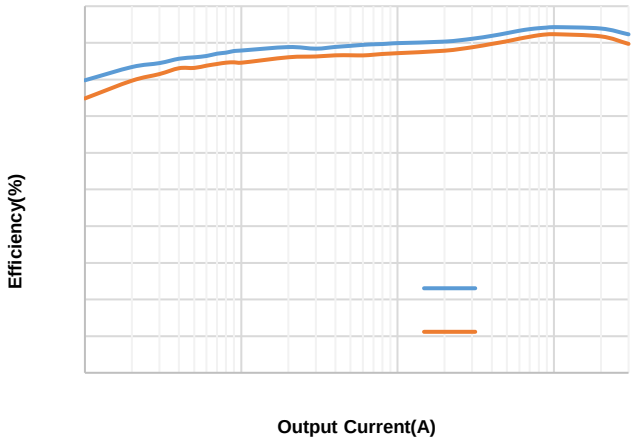


Figure 1. Efficiency vs Load Current

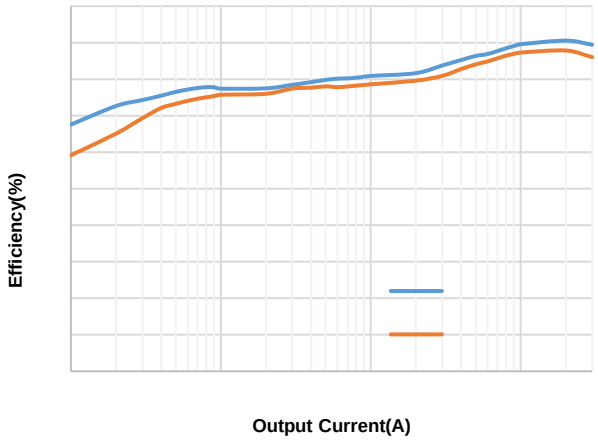


Figure 2. Efficiency vs Load Current

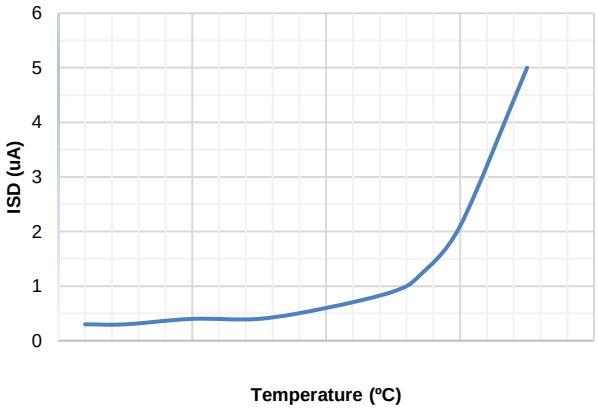


Figure 3. Shut-down Current vs Temperature

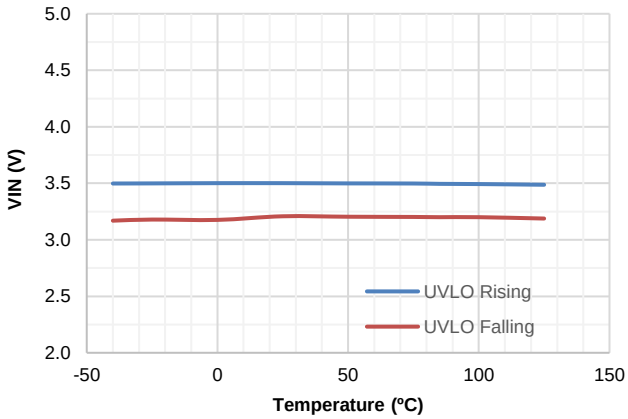


Figure 4. VIN UVLO vs Temperature

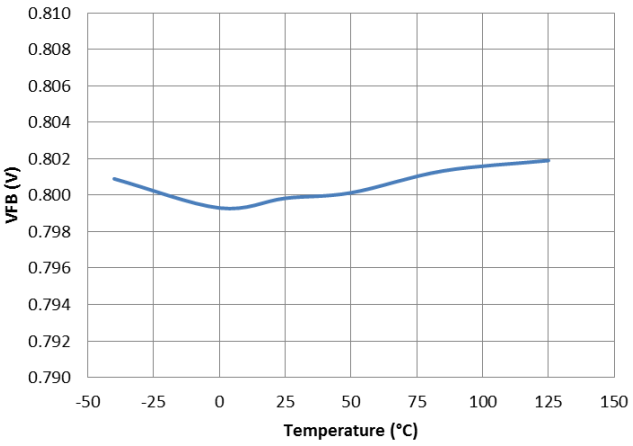


Figure 5. Reference Voltage vs Temperature

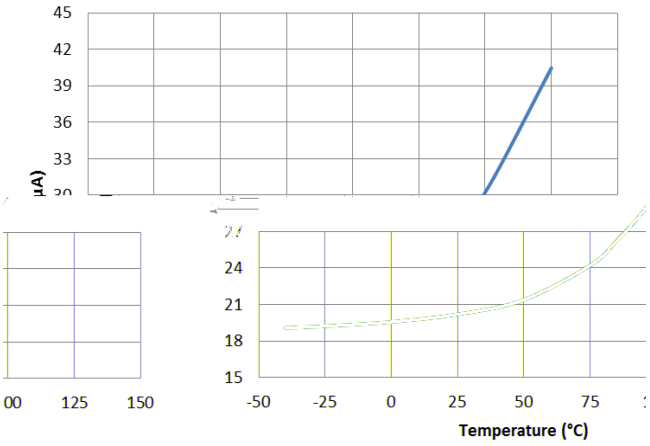
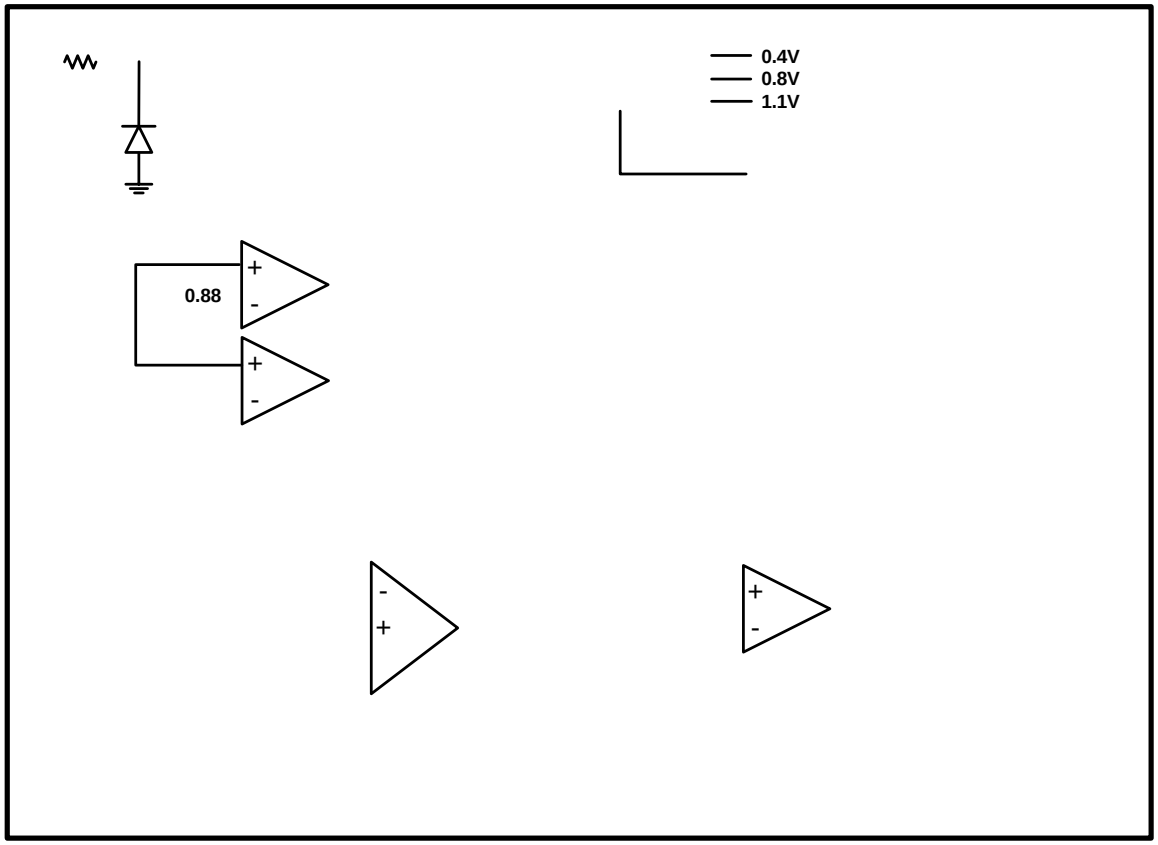


Figure 6. I_Q vs. Temperature, IOUT = 0A



GE PC LA GVL J JMAI GEP K

- CP G

The SCT9431 device is 3.8V-36V input, 3A output, EMI friendly, fully integrated synchronous buck converters. The device employs fixed frequency peak current mode control. An internal clock with 400kHz frequency initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly and the converter charges output cap. When sensed voltage on high-side MOSFET peak current via the CSA block, rising above the voltage of internal COMP (see functional block diagram), the device turns off high-side MOSFET Q1 and turns on low-side MOSFET Q2. The inductor current decreases when MOSFET Q2 is ON. In the next rising edge of clock cycle, the low-side MOSFET Q2 turns off. This repeats on cycle-by-cycle based.

The internal loop compensation network and the built-in 4ms soft-start simplify the SCT9431 footprints, and minimize the off-chip component counts. The quiescent current of SCT9431 is 22uA typical under no-load condition and no switching. When disabling the device, the shutdown current of SCT9431 is only 1μA. The SCT9431 works at Pulse Skipping Mode PSM to further increase the power efficiency in light load condition, hence the power efficiency can be achieved up to 88% at 5mA load condition.

The error amplifier serves the COMP node by comparing the voltage on the FB pin with an internal 0.8V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The SCT9431 device implements Frequency Spread Spectrum (FSS) with a switching frequency jitter of ±6%. FSS reduces EMI by not allowing emitted energy to stay in any one frequency for a significant period of time. The converter further dampens high frequency radiated EMI noise through the use of its proprietary gate driver scheme to achieve a ringing-free switching node voltage without sacrificing the MOSFET switching times.

The hiccup mode minimizes power dissipation during prolonged output overcurrent or short conditions. The hiccup wait time is 512 cycles and the hiccup restart time is 8192 cycles. The SCT9431 device also features protections including cycle-by-cycle high-side MOSFET peak current limit, over-voltage protection, and over-temperature protection.

. 1 5 MFI G.E MBCQ

In heavy load condition, the SCT9431 forces the device operating at PWM mode. When the load current decreasing, the internal COMP net voltage decreases as the inductor current down. With the load current further decreasing, the COMP net voltage decreases and be clamped at a voltage corresponding to the 600mA peak inductor current. When the load current approaches zero, the SCT9431 enter Pulse Skipping Mode (PSM) mode to increase the converter power efficiency at light load condition. When the inductor current decreases to zero, zero-cross detection circuitry on high-side MOSFET Q1 forces the Q1 off till the beginning of the next switching cycle. The buck converter does not sink current from the load when the output load is light and converter works in PSM mode.

4 , . M CP

The SCT9431 is designed to operate from an input voltage supply range between 3.8V to 36V. At least a 0.1uF decoupling ceramic cap is recommended to bypass the supply noise. If the input supply locates more than a few inches from the converter, an additional electrolytic or tantalum bulk capacitor or with recommended 22uF may be required in addition to the local ceramic bypass capacitors.

3LBCP4MJ EC MAI M 34 -

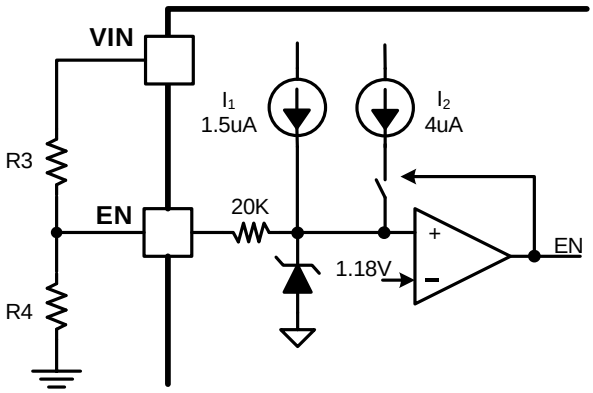
The SCT9431 Under Voltage Lock Out (UVLO) default startup threshold is typical 3.5V with VIN rising and shutdown threshold is 3.1V with VIN falling. The more accurate UVLO threshold can be programmed through the precision enable threshold of EN pin.

L JC LB1 P N

When applying a voltage higher than the EN high threshold (typical 1.18V/rise), the SCT9431 enables all functions and the device starts soft-start phase. The SCT9431 has the built in 4ms soft-start time to prevent the output overshoot and inrush current. When EN pin is pulled low, the internal SS net will be discharged to ground. Buck operation is disabled when EN voltage falls below its lower threshold (typically 1.1V/fall).

An internal 1.5uA pull up current source connected from internal LDO power rail to EN pin guarantees that floating EN pin automatically enables the device. For the application requiring higher VIN UVLO voltage than the default setup, there is a 4uA hysteresis pull up current source on EN pin which configures the VIN UVLO voltage with an off-chip resistor divider R3 and R4, shown in Figure 8. The resistor divider R3 and R4 are calculated by equation (1) and (2).

EN pin is a high voltage pin and can be directly connected to VIN to automatically start up the device with VIN rising to its internal UVLO threshold.



GE FC BHQ JC4 , 34 -

delayed by 220μs to prevent false triggering.

. C I PPCL OK G LB GAA N MBC

The SCT9431 have cycle-by-cycle peak current limit with sensing the internal high side MOSFET Q1 current during overcurrent condition. While the Q1 turns on, its conduction current is monitored by the internal sensing circuitry. Once the high-side MOSFET Q1 current exceeds the limit, it turns off immediately. If the Q1 over current time exceeds 512 switching cycles (hiccup waiting time), the buck converter enters hiccup mode and shuts down. After 8192 cycles off, the buck converter restarts to power up. The hiccup modes reduce the power dissipation in over current condition.

- CP4MJ EC. PMCA GL LB GOK K - L! OK C

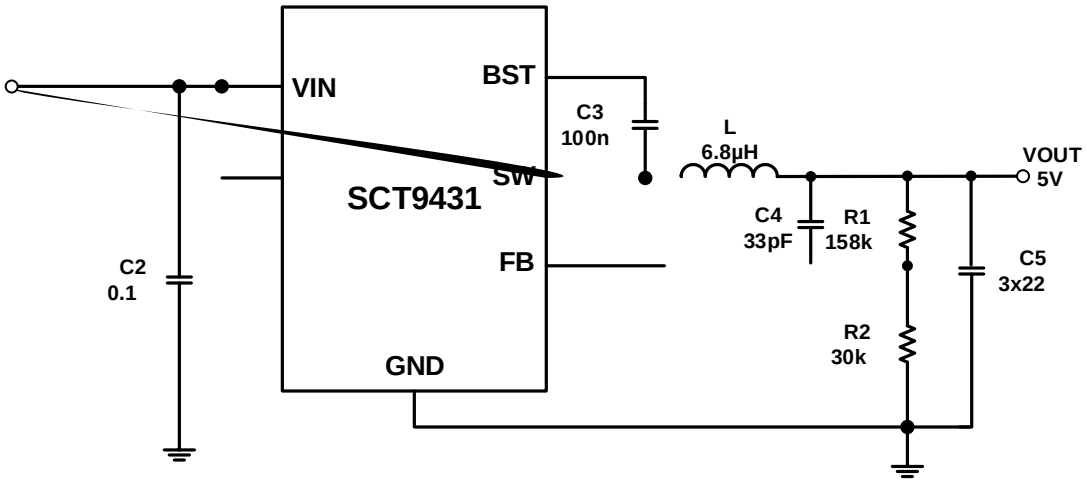
Both SCT9431 feature output over voltage protection ceedsent conditioup mx M ŭ s -te ł

converter. The switching node ringing amplitude and cycles are damped by the built-in MOSFETs gate driving technique (SCT Patented Proprietary Design).

2FCPK J1F BM L

Once the junction temperature in the SCT9431 exceeds 170°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 145°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

2 NCA J NNJCA GML



GE PC 4 LN 4 - N GF L CFL J MK NCLQ GML

CQQEL . P K C CPQ

Design Parameters	Example Value
Input Voltage	12V
Output Voltage	5V
Output Current	3A
Output voltage ripple (peak to peak)	±0.03V
Switching Frequency	400kHz

LN N AGMP1 CJCA G/L

loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss.

- N N AGMP1 C.CA G/L

For buck converter, the output capacitor value determines the regulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

For small output voltage ripple, choose a low-ESR output capacitor like a ceramic capacitor, for example, X5R and X7R family. Typically, 1～2x 22μF ceramic output capacitors work for most applications. Higher capacitor values can be used to improve the load transient response. Due to a capacitor's de-rating under DC bias, the bias can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance.

From the required output voltage ripple, use the equation (6) to calculate the minimum required effective capacitance, C_{OUT}.

(6)

Where

- $V_{OUTRipple}$ is output voltage ripple caused by charging and discharging of the output capacitor.
- ΔI_{LPP} is the inductor peak to peak ripple current, equal to k_{IND} * I_{OUT}.
- f_{SW} is the converter switching frequency.

The allowed maximum ESR of the output capacitor is calculated by the equation (7).

(7)

The output capacitor affects the crossover frequency f_C. Considering the loop stability and effect of the internal loop compensation parameters, choose the crossover frequency less than 40 kHz (—) without considering the feed-forward capacitor. A simple estimation for the crossover frequency without feed forward capacitor is shown in equation (8), assuming C_{OUT} has small ESR.

(8)

Where

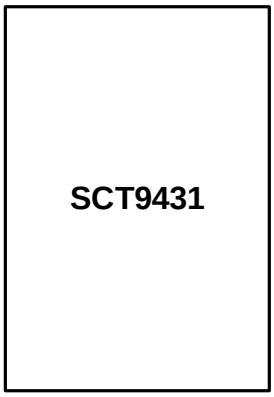
- G_M is the transfer conductance of the error amplifier (300uS).
- G_{MP} is the gain from internal COMP to inductor current, which is 5A/V.
- f_C is the cross over frequency.

Additional capacitance de-rating for aging, temperature and DC bias should be factored in which increases this minimum value. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. The capacitor data sheets specify the RMS (Root Mean Square) value of the maximum ripple current. Equation (9) can be used to calculate the RMS ripple current the output capacitor needs to support.

(9)

- N CCB! MP PB N AGMP1 C.CA G/L

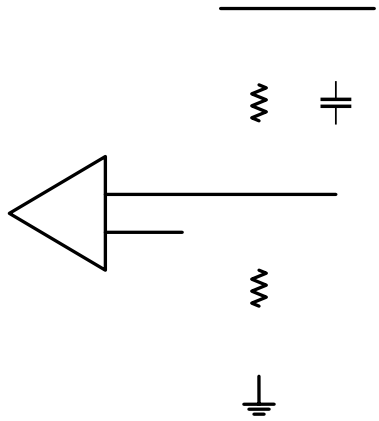
The SCT9431 has the internal integrated loop compensation as shown in the function block diagram. The compensation network includes a 18k resistor and a 7.6nF capacitor. Usually, the type II compensation network has a phase margin between 60 and 90 degree. However, if the output capacitor has ultra-



GE PC 4 LN 4 - N GF CRL J MK NCLQ GVL

Where:

- $T_v(S)$ is the voltage loop
- $T_i(S)$ is the current loop
- $K(S)$ is the voltage sense gain
- $-A_v(S)$ is the feedback compensation gain
- $H_e(S)$ is the current sampling function
- F_m is the PWM comparator gain
- V_{in} is the DC input voltage
- D is the duty cycle
- R_c is the ESR of the output capacitor, COUT
- R_o is the output load resistance$\hat{v}_{in}$ is the AC small-signal input voltage
- $\hat{i}_{in}$ is the AC small-signal input current
- $\hat{d}$ is the modulation of the duty cycle
- $\hat{i}_L$ is the AC small signal of the inductor current
- $\hat{v}_o$ is the AC small signal of output voltage
- $\hat{v}_{comp}$ is the AC small signal voltage of the compensation network



GE FC 2 NC JJ MK NCLQ MP

Transfer function of Figure 12 is expressed in the following equation,

(12)

Where:

The goal of loop compensation design is to achieve:

- High DC Gain
- Gain Margin less than -10dB
- Phase Margin greater than 45°
- Loop Bandwidth Crossover Frequency (f_c) less than 40kHz (10% of f_{sw})

The loop gain at crossover frequency of fc has a unity gain. Therefore, the compensator resistance R3 is determined by equation below. A recommended rule of thumb is to set the crossover frequency to be approximately 1/5 to 1/10 of switching frequency.

(13)

Where

- gm=0.3mS,
- Rt=0.2V/A
- VFB=0.8V,
- fc is the desired crossover frequency
- Vout is the output voltage
- Co is the effective output capacitance.

Be cautioned that most ceramic will degrade with voltage stress or temperature extremes.

The compensator capacitor C6 and C7 are then equal to:

(14)

Where :

- Io is the output load current
- Rc is the ESR equivalent of the Co
- Fs is the switching frequency. In most cases, C7 can omit.

An optional zero, ωz2, can boost the phase margin but it can also increase the gain crossover. Place this zero at 2 to 5 times the fc. Then C4 is equal to:

(15)

2 JC 0CAMK KCLBCB CRL J MK NMLCL Q GF CRL J MK NCLQ G/L

					2k				

NNJA GIL 5 CDVRK Q

Vin=12V, Vout=5V, unless otherwise noted

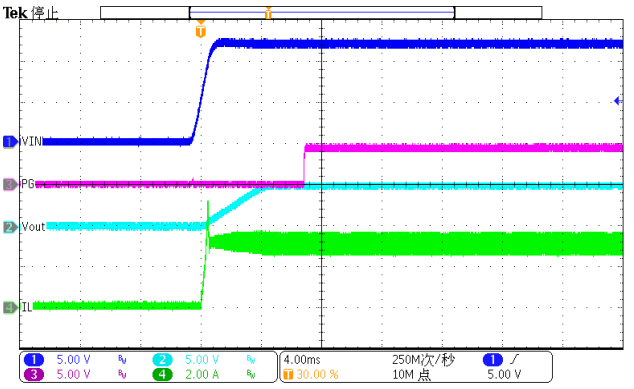


Figure 13. Power up(Iload=3A)

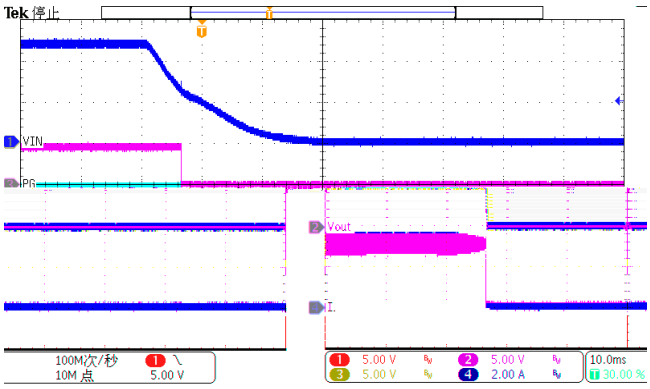


Figure 14. Power down(Iload=3A)

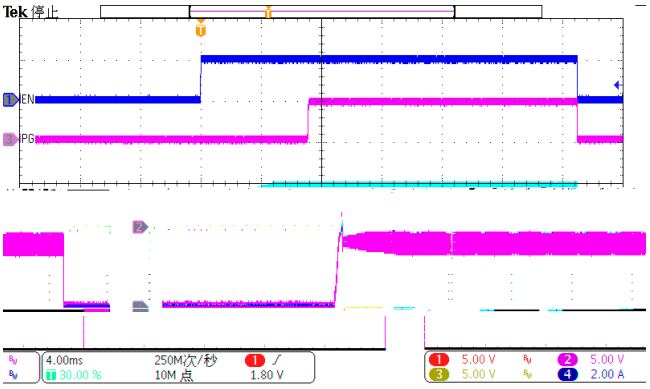


Figure 15.Enable (Iload=3A)

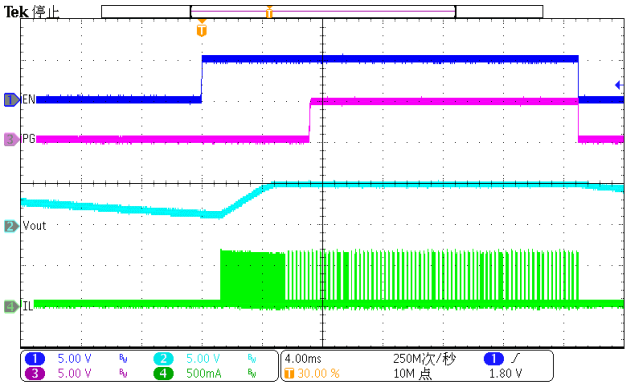


Figure 16. Enable (Iload=10mA)

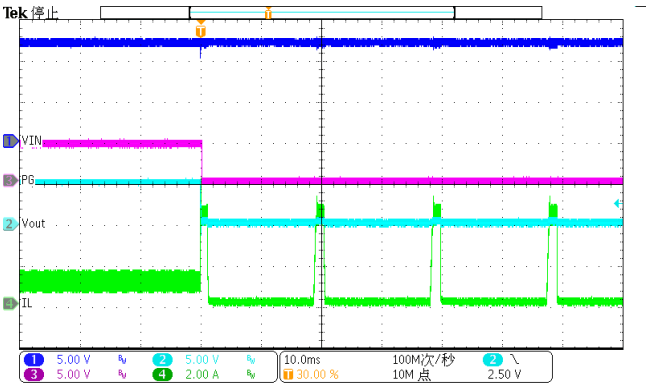


Figure17. Normal to Hard Short

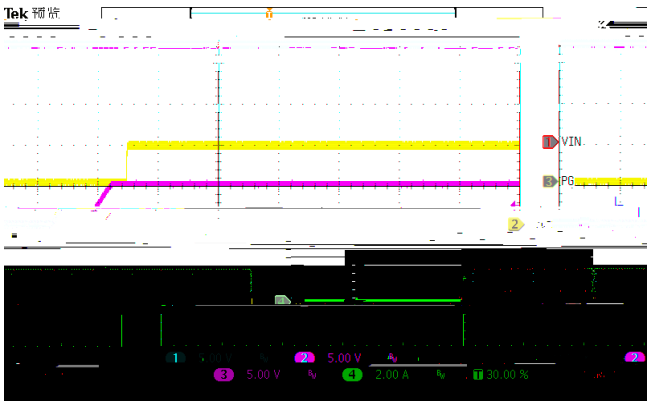


Figure 18. Hard Short Recovery

NNJA GML 5 CDMRK Q AML G CB

Vin=12V, Vout=5V, unless otherwise noted

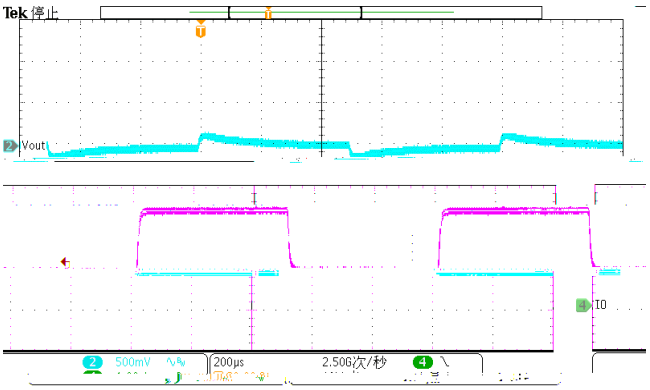


Figure 19. Load Transient (0.75A-2.25A, 1.6A/us)

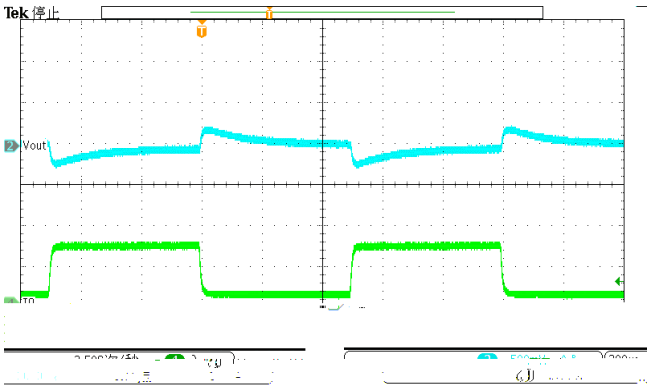


Figure 20. Load Transient (0.3A-2.7A, 1.6A/us)

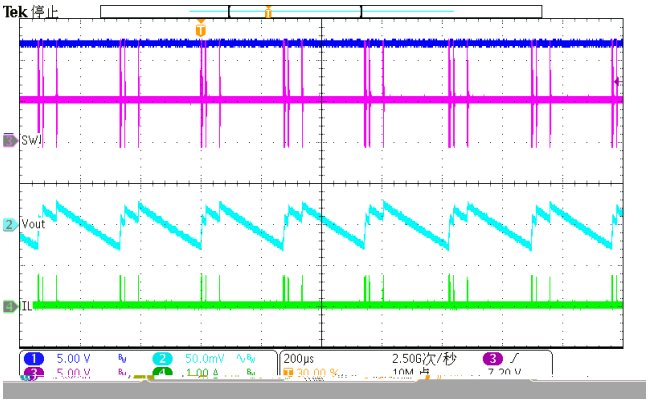


Figure 21. Output Ripple (Iload=10mA)

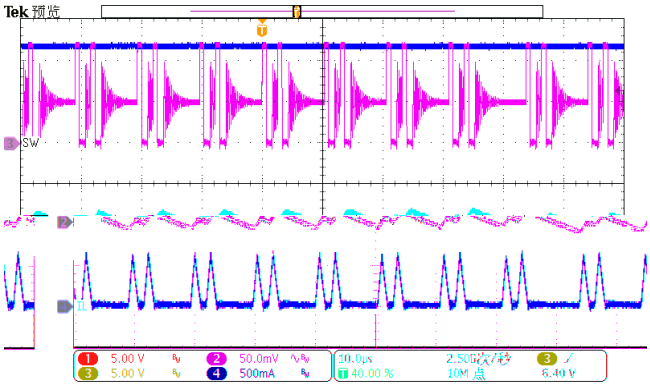


Figure 22. Output Ripple (Iload=0.1A)

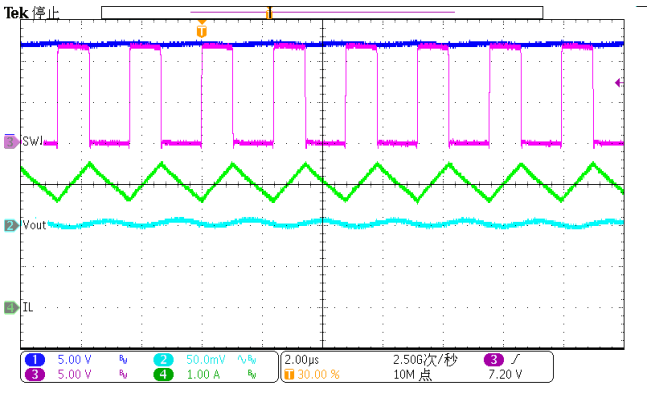


Figure 23. Output Ripple (Iload=3A)

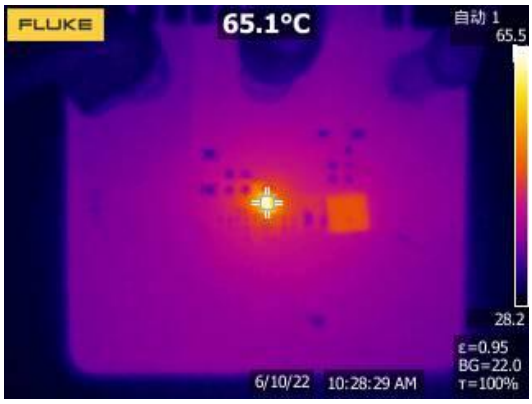


Figure 24. Thermal, 12VIN, 5Vout, 3A

M % GBCJLC

Figure 25 and Figure 26 are the recommended PCB layout of SCT9431 with or without external compensation network.

1. The SCT9431 works at 3A load current so heat dissipation is a major concern in the layout of the PCB. 2oz copper for both the top and bottom layers is recommended.
2. Place the input capacitors as closely across VIN and GND as possible.
3. Place the inductor as close to SW as possible.
4. Place the output capacitors as close to GND as possible.
5. Place the feedback components as close to FB as possible.
6. If using four or more layers, use at least the 2nd and 3rd layers as GND to maximize thermal performance.
7. Add as many vias under both the thermally exposed GND pad and GND plane for heat dissipation to all the GND layers.
8. Add as many vias under both the thermally exposed VIN pad and VIN plane for heat dissipation to all the VIN layers.

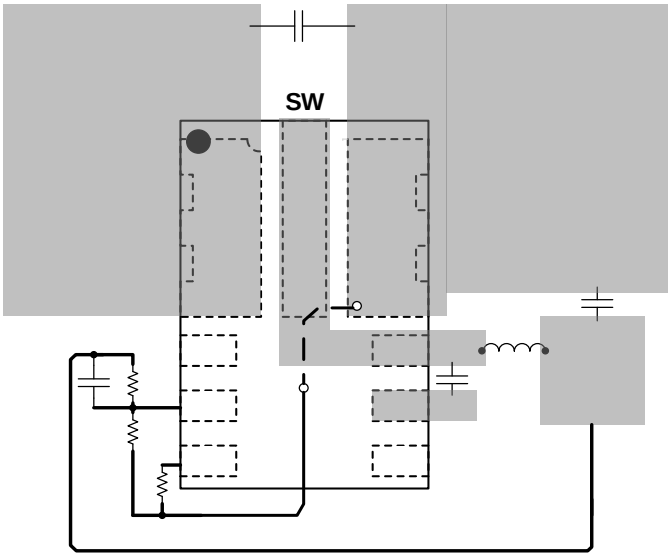


Figure 25. PCB Layout Example for application with internal compensation

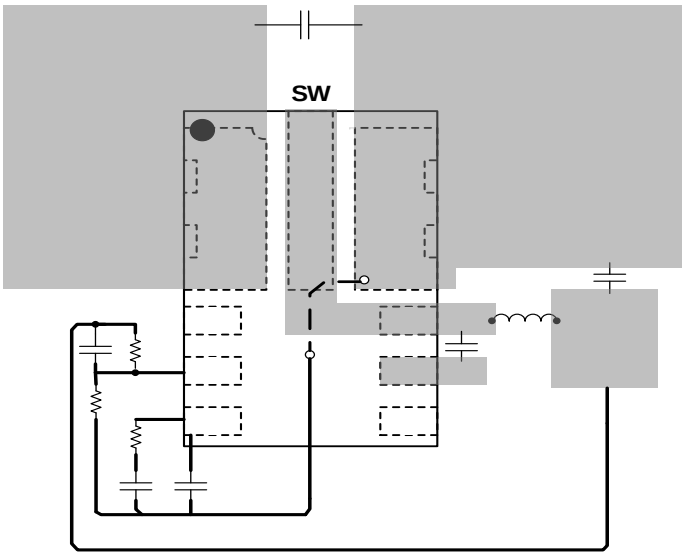
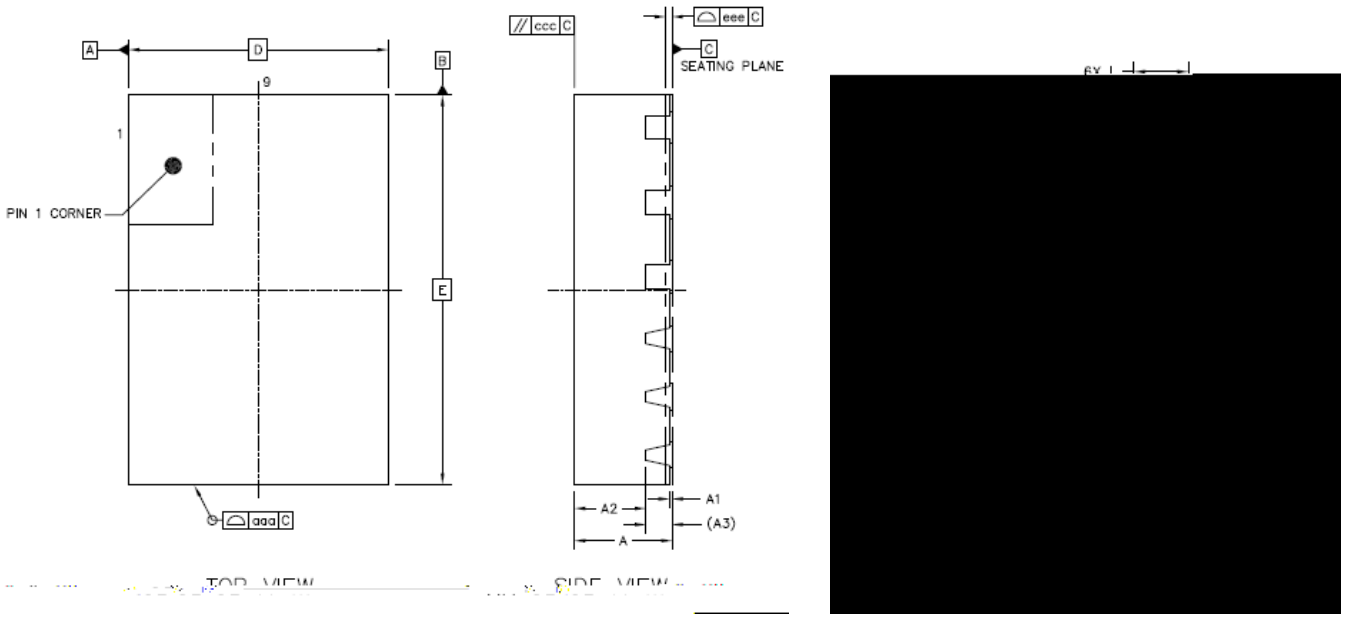


Figure 26. PCB Layout Example for application with external compensation



FCQFN-9L (2*3) Package Outline Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	---	0.55	---
A3		0.203 REF	
b	0.15	0.2	0.25
b1	0.2	0.25	0.3
b2	0.25	0.3	0.35
D		2 BSC	
E		3 BSC	
e		0.45 BSC	
e1		0.475 BSC	
e2		0.575 BSC	
e3		0.1 BSC	
L	0.35	0.40	0.45
L1	0.55	0.6	0.65
L2	1.475	1.525	1.575
L3		0.15 REF	
aaa		0.1	
ccc		0.1	
eee		0.05	
bbb		0.1	

, - 2

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

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