V

- Synchronous DCDC Buck Controller
  - 5.5V-100V Wide Input Range
  - 0.8V-60V Adjustable Output Voltage
  - 0.8V±1% Reference Voltage
  - 40ns Minimum $t_{ON}$ for low duty ratio
  - 140ns Minimum $t_{OFF}$ for high duty ratio
- 100 KHz to 1.2 MHz Switching Frequency
  - Clock Synchronization In/Out capability
  - Selectable Diode Emulation or FPWM
- 7.5-V Gate Drivers
  - 2.3-A Source and 3.5-A Sink Current
  - Low-side Soft Start for prebiased Start-up
- Fast Line and Load Transient Response
  - Voltage-mode control with line feedforward
  - High Gain Bandwidth Error Amplifier
- Protection Features for Robustness
  - Adjustable Soft Start time
  - Hiccup-mode Overcurrent Protection
  - Input UVLO with hysteresis
  - VCC and Gate-drive UVLO Protection
  - Precision Enable Input Threshold
  - Open-drain Power Good Indicator for Sequencing and Control
  - Over Temperature Shutdown Protection
- External VCC Input for Bypassing Internal LDO
- Available in QFN-20L 3.5mmx4.5mm Package

- High Current Distributed Power Systems
- Telecom, Datacom

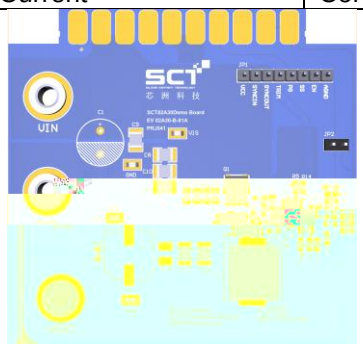
with wide input voltage (wide VIN) range, wide duty cycle range, voltage-mode PWM control loop, integrated high-side and low-side MOSFET gate drivers, cycle-by-cycle overcurrent protection, precision enable, and power supply tracking features. The EVM's free-running switching frequency is 400 kHz and is synchronizable to a higher or lower frequency if required. Moreover, a synchronization output signal (SYNCOUT) 180° phase-shifted relative to the internal clock is available for master-slave configurations. VCC voltage rail UVLO protects the converter at low input voltage conditions, and the EN/UVLO pin supports adjustable input UVLO for application specific power-up and power-down requirements.

The device is available in QFN-20L 3.5mmx4.5mm Package

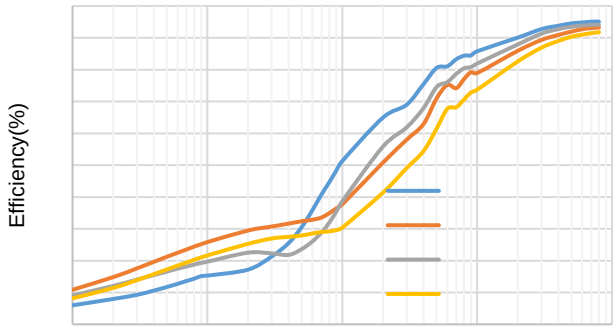
This user's guide describes the characteristics, operation and the use of the EV82A30-B-01A Evaluation Module including EVM specifications, recommended test setup, test result, schematic diagram, bill of materials, and the board layout.

| Board Number | IC Number |
|---|---|
| EV82A30-B-01A | SCT82A30 |

| Parameter | Condition | Value |
|---|---|---|
| Input Voltage | DC up to 85V | 15V-85V |
| Output Voltage | Iout=0A~8A | 12V ± 1% |
| Output Current | Continuous DC current | 8A |



EV82A30-B-04A Evaluation Board Top View




SCT82A30 Efficiency, Freq.=400KHz

Evaluation board EV82A30-B-01A is easy to set up to evaluate the performance of SCT82A30 synchronous step-down DCDC converter. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

1. Place jumpers in the following positions:
   - VIN,GND : Connect the power supply to the input of converter.
   - VOUT,GND : Connect the load to the output of converter.
   - VIS: Input voltage test point.
   - VOS: Output voltage test point.
   - JP1:VCC,SYNCIN,SYNCOUT,TRIM,PG,SS,EN,AGND Pin connector.
   - JP2: Connect Extvcc and Vout.
2. With power off, connect the input power supply to $V_{IN}$ connector and GND connector. Make sure that the input voltage does not exceed 85V, and supports sufficient current limit. Turn on the power at the input.
3. Check the output voltage at VOS,GND. The output voltage should be 12V typical. Once the proper output voltage is established, adjust the load within the operating range and observe the output voltage regulation, output voltage ripple, efficiency and other parameters.
4. To use the enable function, apply a digital input to the EN pin of JP1.
5. Trim input for output voltage adjust.
6. Users can place C1 if input wire is long and C24 for better load transient performance.

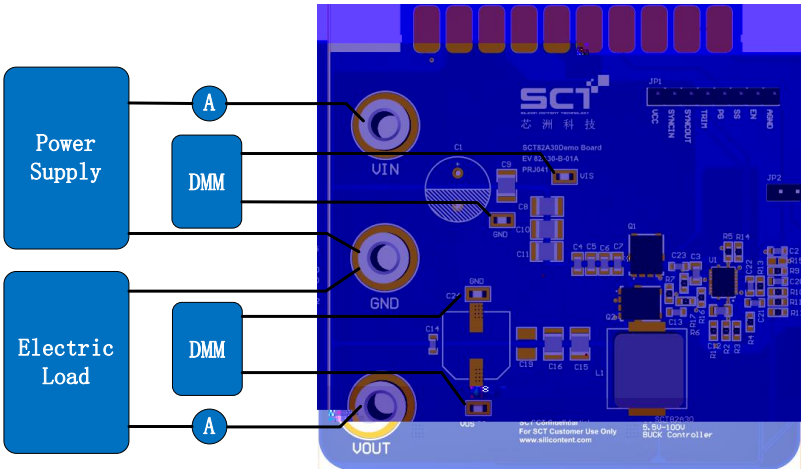



Figure 1. Power Supply, Load and Measurement Equipment Setup

NOTE: When measuring the voltage ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. Measure the input or output voltage ripple by touching the probe tip directly across relevant capacitor of VIN or VOUT. See Figure 2 for proper scope probe technique.


Figure 2. Measuring Voltage Ripple across Terminals or Directly Across Ceramic Capacitor

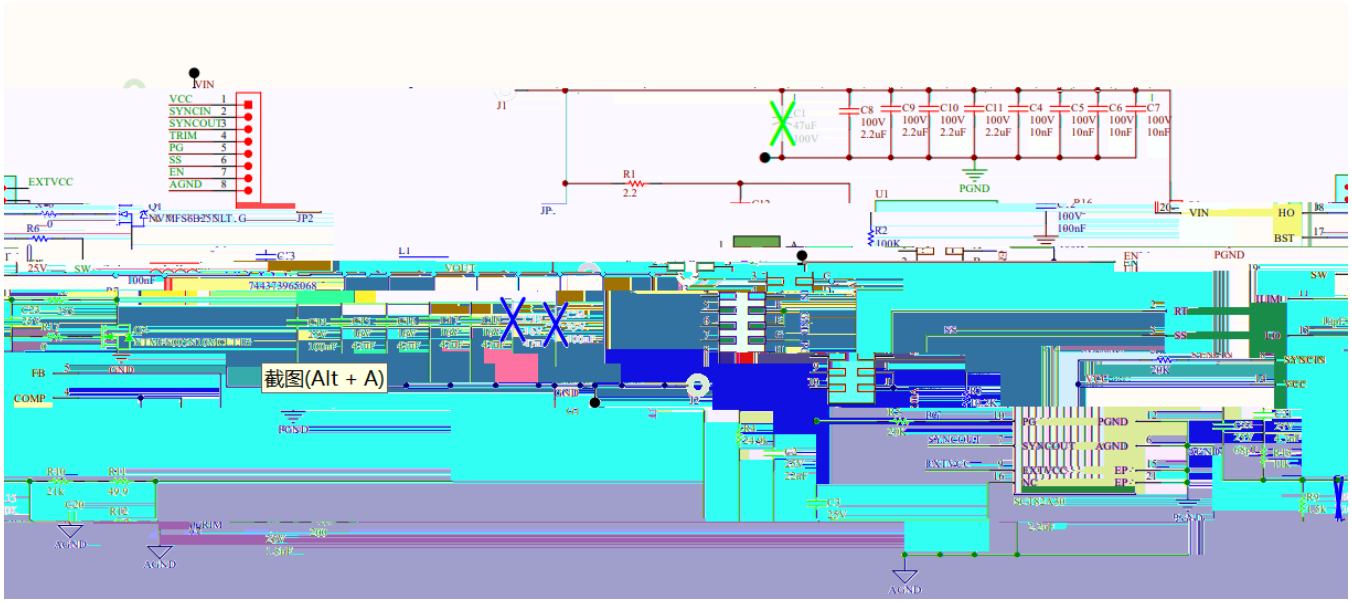



Figure 3. SCT82A30 EVM Schematic

Table 2. SCT82A30 EVM Bills of Materials

| Manufacture | Part Number | Designator |
|---|---|---|

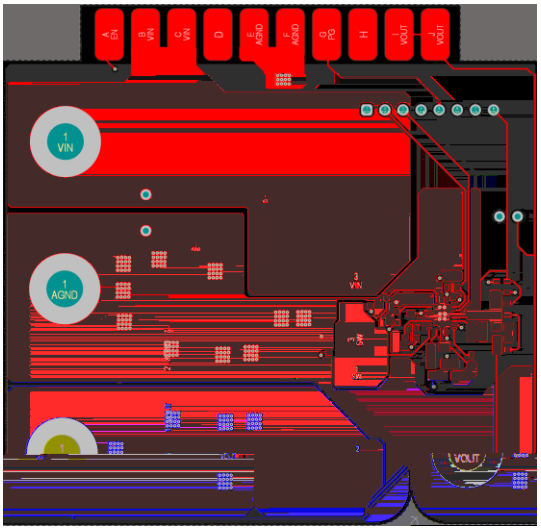



Figure 4. Top Layer

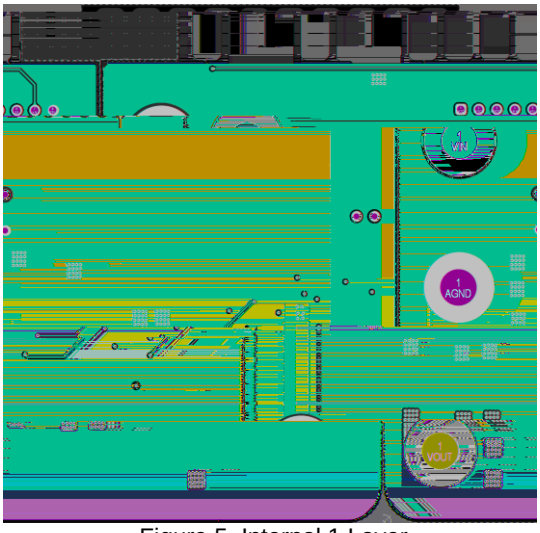



Figure 5. Internal 1 Layer

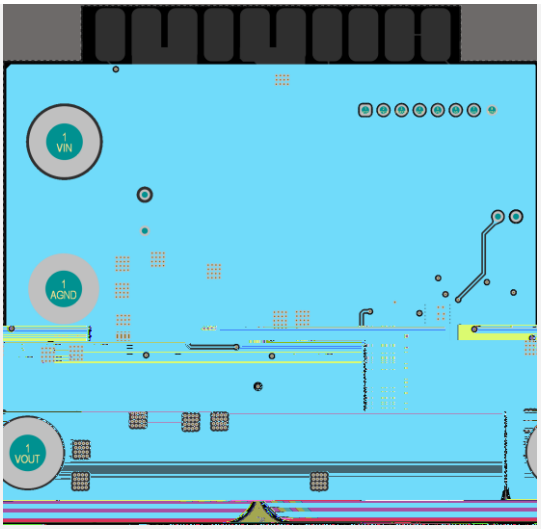



Figure 6. Internal 2 Layer

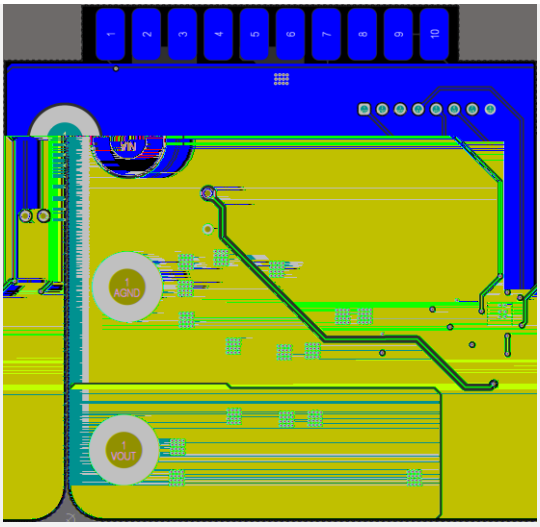



Figure 7. Bottom Layer

Vin=48V, Vout=12V, unless otherwise noted

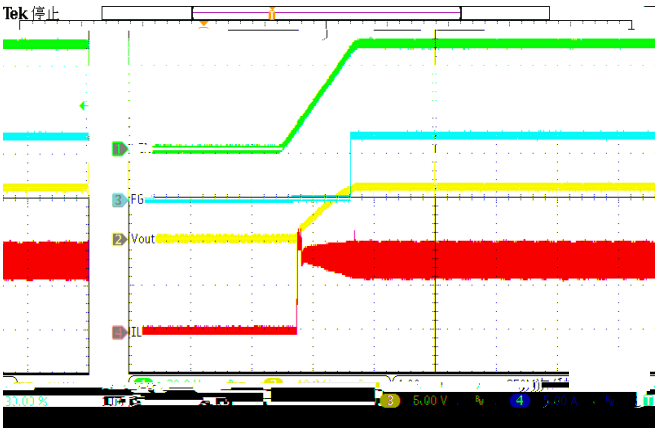



Figure 8. Power Up
(CH-1: Vin, CH-2: Vout, CH-3: PG, CH-IL)

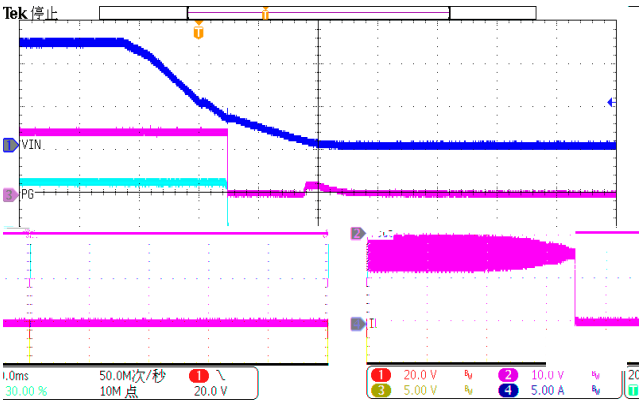



Figure 9. Power Down
(CH-1: Vin, CH-2: Vout, CH-3: PG, CH-IL)

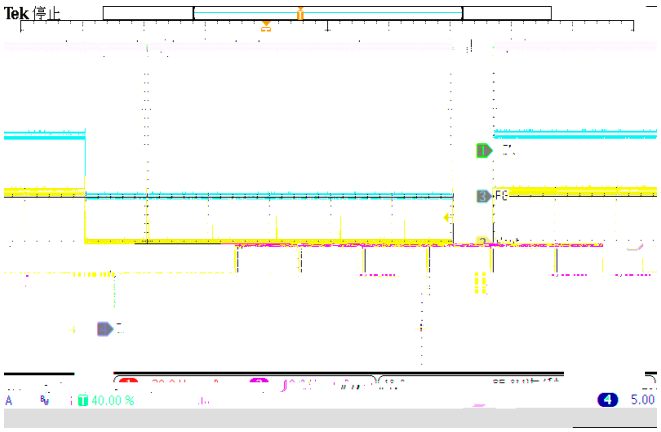



Figure 10. Startup at Output Hard-short
(CH-1: Vin, CH-2: Vout, CH-3: PG, CH-IL)

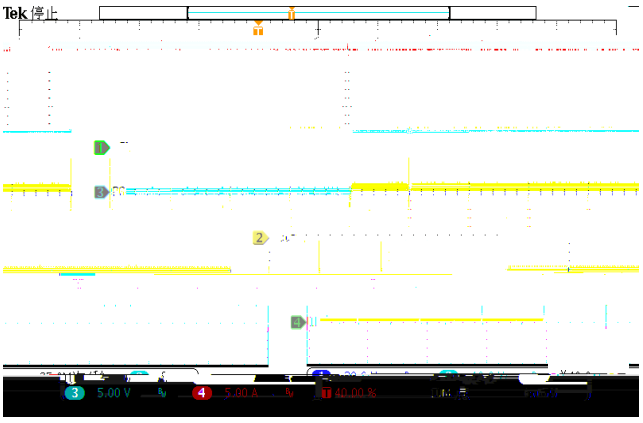



Figure 11. Output Hard-short and Recovery
(CH-1: Vin, CH-2: Vout, CH-3: PG, CH-IL)

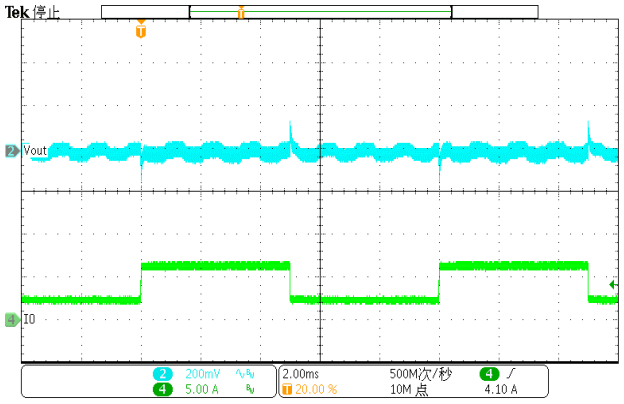



Figure 12. Load Transient
(2A-6A, SR=1600mA/us, CH-4: Iout, CH-2: Vout)

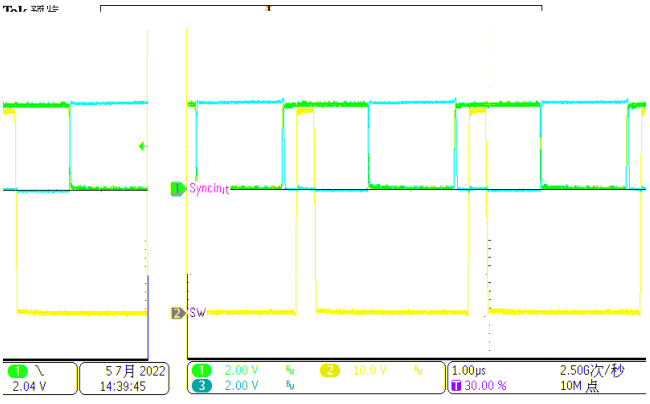



Figure 13. SYNCIN and SYNCOUT
(CH-1: SYCNIN, CH-2: SW, CH-3: SYNCOUT)

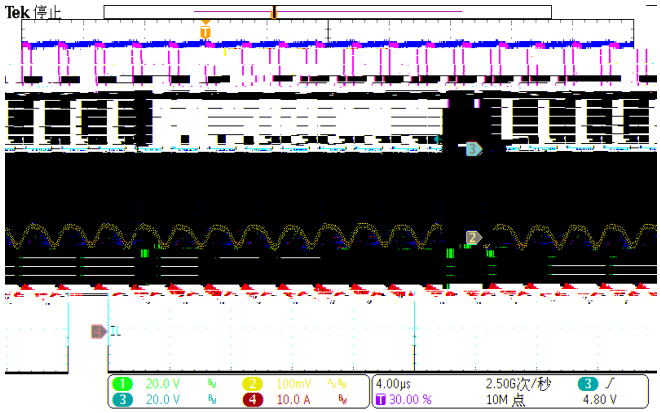



Figure 14.
(CH-1: Vin, CH-2: Vout, CH-3: SW, CH-4: IL)

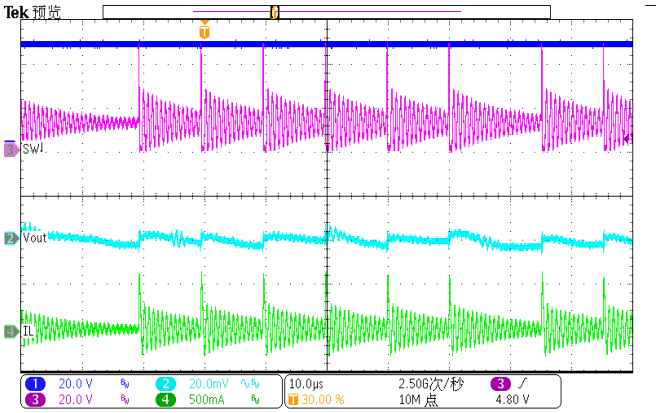



Figure 15.
(CH-1: Vin, CH-2: Vout, CH-3: SW, CH-4: IL)

### Overcurrent Protection

The EVM implements current sense schemes , using the on-state resistance of the low-side MOSFET, limiting the inductor current during an overload or output short-circuit condition. The controller senses the inductor current during the PWM off-time when LO is high.

If an application requires a higher current, R7 can be used to achieve an expected system current. The current limit threshold can be calculated by Equation 4.

(4)

### Under Voltage Lockout Threshold

The SCT82A30 are enabled when the VIN pin voltage rises about 5.5V and the EN pin voltage exceeds the enable threshold of 1.2V.

If an application requires a higher system under voltage lockout threshold, two external resistors divider (R2 and R3) in Figure 16 can be used to achieve an expected system UVLO. The UVLO rising and falling threshold can be calculated by Equation 5 and Equation 6 respectively.

where:

- $V_{IN(ON)}$ is the rising threshold of Vin UVLO.
- $V_{IN(OFF)}$ is the falling threshold of Vin UVLO

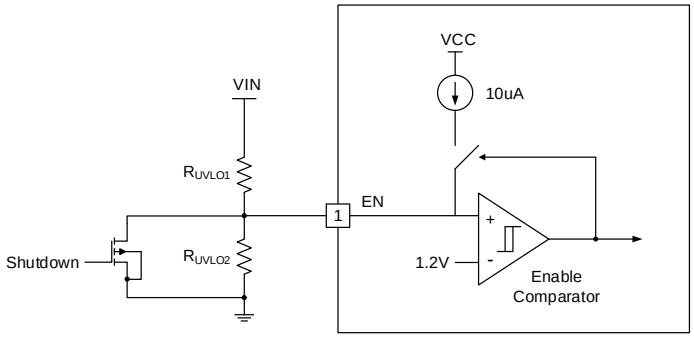



Figure 16. VIN UVLO Programmable by EN Dividers

## IMPORTANT NOTICE

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**Silicon Content Technology Co., Ltd.**
#1 Floor 2 Building 15, Yard 33 Dijin Road, Haidian District, Beijing 100095
(86 10) 64779806 FAX: (86 10) 64779806 www.silicontent.com