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- Wide Input Voltage Range: 2.7V-12V
- Wide Output Voltage Range: 4.5V-12.6V
- Fully Integrated 17t ƒ 'Opmo'Zpkl 'ML 'huk' 14t ƒ 'Sv~'Zpkl 'ML
- Up to 93% Efficiency at Vin=3.3V, Vout=9V, and Iout=2A
- Programmable and Up to 9.5A Peak Switch Current Limit
- Typical Shut-down Current: 1uA
- Adjustable Switching Frequency: 200KHz to 2.2MHz
- Forced PWM Operation Mode at Light Load
- Internal Soft Start and External Compensation
- Cycle-by-Cycle Overcurrent Protection
- Output Overvoltage Protection
- Thermal Shutdown Protection: 160°C
- QFN-11 2mm x 2.5mm Package

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- Bluetooth Speaker
- Portable POS Terminal
- Quick Charge Power Bank
- E-Cigarette
- Outdoor Flashlight

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The SCT1270F is a high efficiency synchronous boost converter with fully integrated a 17t ƒ high-side MOSFET and a 14t ƒ low-side MOSFET, featuring 2.7V to 12V input voltage range to support single cell or two cell Lithium ion/polymer batteries and up to 9.5A peak switch current. The switch current limit can be adjustable with an external resistor. The SCT1270F has 7A continuous switch current capability and provides output voltage up to 12.6V.

The SCT1270F adopts constant off-time peak current control to provide fast transient response. An external compensation network allows flexibility setting loop dynamics to achieve optimal transient performance at different load conditions.

The SCT1270F works in the PWM at moderate and heavy load condition and also works in the PWM mode at light load to avoid application problems caused by low switching frequency. The switching frequency is adjustable from 200KHz to 2.2MHz.

The SCT1270F features output overvoltage protection and thermal shutdown protection when the device over loads.

The device is available in a QFN-11 2mm x 2.5mm package.

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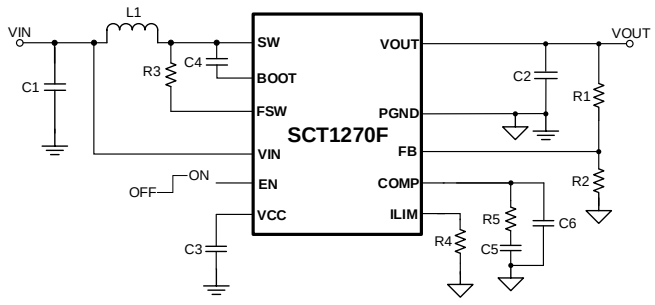
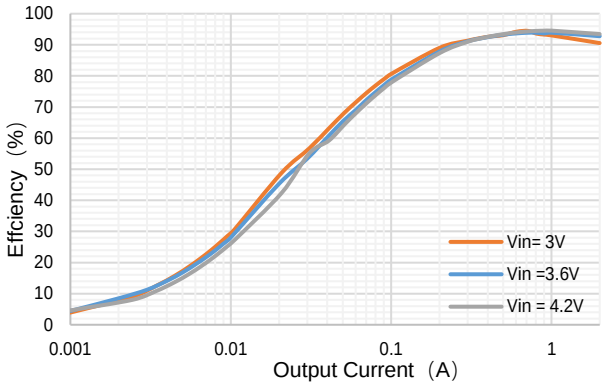




Efficiency vs Load Current, Vout=9V

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Production

Revision 1.1: Update T_J to 150 ºC

Revision 1.2: Update DEVICE ORDER INFORMATION

ORDERING INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT1270FFQAR	Tape & Reel	3000	270F	11	11-Lead 2mm×2.5mm Plastic QFN

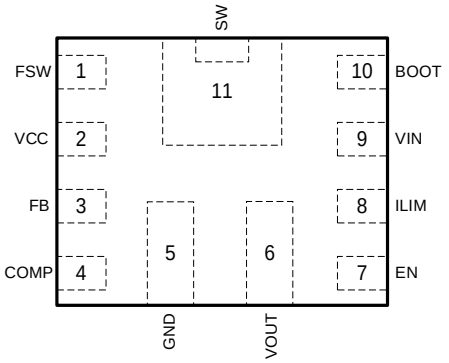
ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
BOOT	-0.3	21.5	V
VIN, SW, FSW, VOUT	-0.3	14.5	V
SW (<20ns)	-1.5	16.5	V
VCC, LIM, FB, EN, COMP, MODE	-0.3	5.5	V
BOOT-SW	-0.3	5.5	V
Operating ambient temperature T_A	-40	125	ºC
Operating junction temperature T_J(2)	-40	150	ºC
Storage temperature T_{STG}	-65	150	ºC

PIN DIAGRAM

Top View: 11-Lead Plastic QFN 2mm x 2.5mm



(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
FSW	1	Place a resistor from this pin to SW to sets the switching frequency.
VCC	2	Internal linear regulator output. Connect a 1uF or larger ceramic capacitor to ground. VCC can not to be externally driven. No additional components or loading is recommended on this pin.
FB	3	Feedback Input. Connect a resistor divider from VOUT to FB to set up output voltage.
COMP	4	Output of the error amplifier and switching converter loop compensation point.
GND	5	Ground
VOUT	6	Boost converter output. Connect a 1uF decoupling capacitor as close to VOUT pins and power ground pad as possible to reduce the ranging voltage of SW.
EN	7	Enable logic input. An 757R 'y zpz vyconnects this pin to ground inside. Floating disables the device.
ILIM	8	Inductor peak current limit set point input. A resistor connecting this pin to ground sets current limit through low-side power FET.

VIN	9	Power supply input. Must be locally bypassed with a capacitor as close as possible to the pin.
BOOT	10	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BOOT pin and SW node.
SW	11	Switching node of the boost converter.

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Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	2.7	12	V
V_{OUT}	Output voltage range	4.5	12.6	V
T_J	Operating junction temperature	-40	150	°C

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PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(2)	-0.5	+0.5	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

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PARAMETER	THERMAL METRIC	QFN-11L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	53.4	°C/W
$R_{\theta JC}$	Junction to case thermal resistance(1)	59.2	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT1270F is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT1270F. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

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V_{IN}=3.6V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		2.7		12	V
V_{OUT}	Output voltage range		4.5		12.6	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising		2.5 200		V mV
I_{SD}	Shutdown current	EN=0, no load and measured on VIN pin		1		uA
I_Q	Quiescent current from VIN	EN=2V, no load, no switching		1.8		uA
	Quiescent current from VOUT			450		uA
V_{CC}	Internal linear regulator	I_{VCC}=5mA, V_{IN}=6V		4.75		V
V_{CC_UVLO}	VCC UVLO threshold	V_{IN} falling		2.2		V
Reference and Control Loop						
V_{REF}	Reference voltage of FB		0.98	1	1.02	V
I_{FB}	FB pin leakage current	V_{FB}=1V			100	nA
G_{EA}	Error amplifier trans-conductance	V_{COMP}=1.5V		200		uS
I_{COMP_SRC}	Error amplifier maximum source current	V_{FB}=V_{REF}-200mV, V_{COMP}=1.5V		24		uA
I_{COMP_SNK}	Error amplifier maximum sink current	V_{FB}=V_{REF}+200mV, V_{COMP}=1.5V		24		uA
V_{COMP_H}	COMP high clamp	V_{FB}=0.8V, R_{ILIM}=100r *f*		2.2		V
V_{COMP_L}	COMP low clamp	V_{FB}=1.2V, R_{ILIM}=100r *f* , PFM		0.9		V
Power MOSFETs						
R_{DSON_H}	High side FET on-resistance			17		t *f*
R_{DSON_L}	Low side FET on-resistance			14		t *f*
Current Limit						
I_{LIM}	Peak current limit	R_{ILIM}=100r *f*	7.2	8	8.8	A
		R_{ILIM}=84r *f*		9.5		A
Enable						
V_{EN}	Enable high threshold Enable low threshold		 0.4		1.2	V V
R_{EN}	Enable pull down resistance			750		r *f*
T_{SS}	Soft-start Current			4		ms
Switching Frequency						
F_{SW}	Switching frequency	R_{FSW}=308r *f* , V_{OUT}=12V		500		kHz
t_{ON_MIN}	Minimum on-time	R_{FSW}=308r *f* 3 $_{OUT}$=12V		170		ns
Protection						
V_{OVP_VOUT}	Output overvoltage threshold Hysteresis	VOUT rising		13.2 280		V mV
T_{SD}	Thermal shutdown threshold	T_J rising		164		°C
	Hysteresis			24		°C

*Derived from bench characterization

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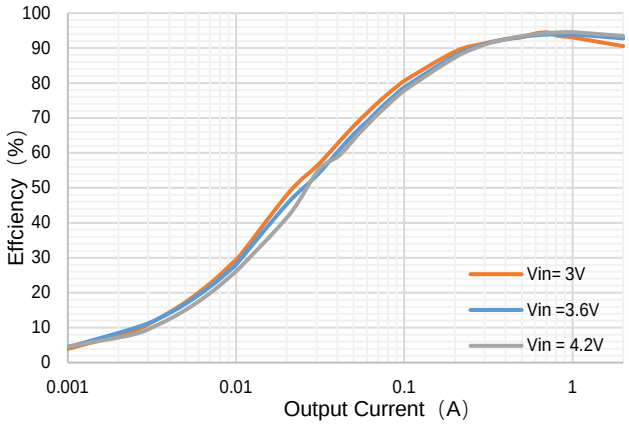

Figure 1. SCT1270F Efficiency vs Load Current, Vout=9V

Figure 2. SCT1270F Efficiency vs Load Current, Vin=3.6V

Figure 3. Load Regulation (Vin=3.6V, Vout=9V)

Figure 4. Line Regulation, Vout=9V

Figure 5. Current Limit VS Setting Resistance

Figure 6. Switching Frequency VS Setting Resistance

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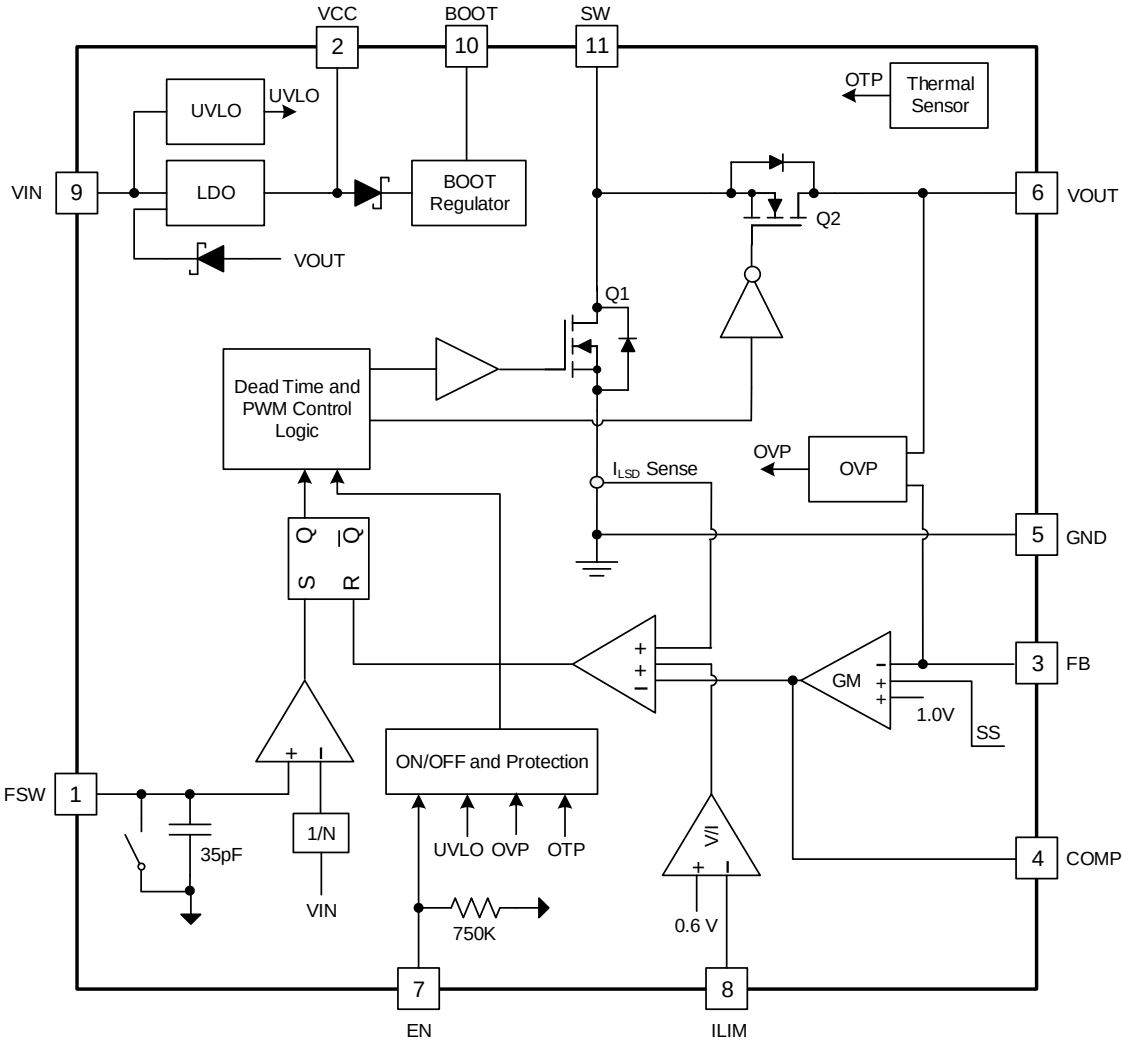

Figure 7. Functional Block Diagram

the device.

The SCT1270F features fixed 4ms soft start to prevent inrush current during power-up.

Adjustable Peak Current Limit

The SCT1270F boost converter implements cycle-by-cycle peak current limit function with sensing the internal low-side power MOSFET Q1 during overcurrent condition. While the Q1 is turned on, its conduction current is monitored by the internal sensing circuitry. Once the low-side MOSFET Q1 current exceeds the limit, it turns off immediately. An external resistor connecting ILIM pin to ground sets the low-side MOSFET Q1 peak current limit threshold. Use Equation 1 or Figure 5 to calculate the peak current limit.

$$C \qquad \frac{2}{L} \tag{1}$$

where:

- I_{LIM} is the peak current limit
- R_{LIM} is the resistance between ILIM pin to ground.

This current limit function is realized by detecting the current flowing through the low-side MOSFET. The current limit feature loses function in the output hard short circuit conditions. At normal operation, when the output hard shorts to ground, there is a direct path to short the input voltage through high-side MOSFET Q2 or its body diode even the Q2 is turned off. This could damage the circuit components and cause catastrophic failure at load circuit.

Adjustable Switching Frequency

The SCT1270F features a wide adjustable switching frequency ranging from 200kHz to 2.2MHz. The switching frequency is set by a resistor connected between the FSW pin and the SW pin of SCT1270F. Do not leave the FSW pin open. Use Equation 2 to calculate the resistor value required for a desired frequency.

$$L \qquad \frac{0 \quad — \qquad —}{} \tag{2}$$

where:

- f_{SW} is the desired switching frequency
- T_{DELAY} = 70 ns
- C_{FREQ} = 35 pF
- V_{IN} is the input voltage
- V_{OUT} is the output voltage

Over Voltage Protection and Minimum On-time

The SCT1270F features VOUT pin over voltage protection. If the VOUT pin is above 13.2V typical, the device stops switching immediately until the VOUT pin drops below 12.92V. The OVP function prevents the connected output circuitry from un-predictive overvoltage.

The low-side MOSFET has minimum on-time 170ns typical limitation. While the device is operating at minimum on time and further increasing Vin push output voltage beyond regulation point. With output and feedback over voltage protection, the converter skips pulse with turning off high-side MOSFET and prevents output running higher to damage the load.

Forced PWM Mode

In the forced PWM mode, the SCT1270F keeps the switching frequency unchanged in light load condition. When the load current decreases, the output of the internal error amplifier decreases as well to keep the inductor peak current down, delivering less power from input to output. When the output current further reduces, the current through the inductor will decrease to zero during the off-time. The high-side N-MOSFET is not turned off even if the current through the MOSFET is zero. Thus, the inductor current changes its direction after it runs to zero. The power flow is from output side to input side. The efficiency will be low in this mode. But with the fixed switching frequency,

there is no audible noise and other problems which might be caused by low switching frequency in light load condition.

Thermal Shutdown

Once the junction temperature in the SCT1270F exceeds 164 C, the thermal sensing circuit stops switching until the junction temperature falling below 140 C, and the device restarts. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

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Typical Application

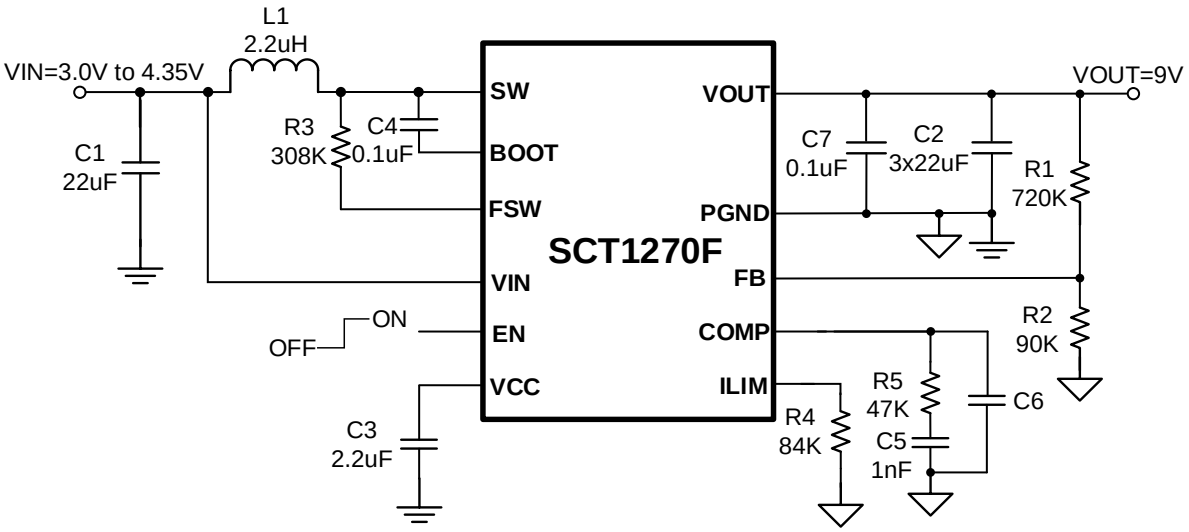

Figure 8. One Cell Battery Input, 9V/2A (20W) Output

Switching Frequency

The resistor connected from FSW to SW sets switching frequency of the converter. The resistor value required for a desired frequency can be calculated using equation 3. High frequency can reduce the inductor and output capacitor size with the tradeoff of more thermal dissipation and lower efficiency.

$$L \quad \frac{0 \quad — \qquad —}{} \qquad (3)$$

where:

- f_{SW} is the desired switching frequency
- T_{DELAY} = 70 ns
- C_{FREQ} = 35 pF
- V_{IN} is the input voltage
- V_{OUT} is the output voltage

Fsw	R_{FREQ}
200 KHz	830 R
350 KHz	467' R
520 KHz	300 R
850 KHz	162 R
1000 KHz	140 R
2000 KHz	55 R

Peak Current Limit

Using the correct external resistor at ILIM pin sets the peak input current. Table 2 shows the resistor value for inductor peak current limit. For a typical current limit of 9.5A, the resistor value is 84R . The minimum current limit must be higher than the required peak switch current at lowest input voltage and the highest output power not to hit the current limit and still regulate the output voltage.

$$C \quad \frac{2}{L} \qquad (4)$$

where:

- I_{LIM} is the peak current limit
- R_{LIM} is the resistance of ILIM pin to ground

Inductor Selection

The performance of puk j vy'hmmhj z' ol 'ww~l y'z wws z'z l hk 'z h l 'vwl yh pvu3 yhuzpb u 'i l oh pvy3svvw'z hi psp 3 and boost converter efficiency. The inductor value, DC resistance, and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DC resistance, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, maxim load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a boost converter, calculate the inductor DC current as in equation 6

$$C \quad \frac{P \quad C}{P} \tag{6}$$

Where

- V_{OUT} is the output voltage of the boost converter
- I_{OUT} is the output current of the boost converter
- V_{IN} is the input voltage of the boost converter
- 'pz' ol 'ww~l y'jvu l yzpvu'l mpjpb uj

Calculate the inductor current peak-to-peak ripple, I_{LPP}, as in equation 7

$$C \quad \frac{5}{\_\_\_\_\_ \quad \_\_} \tag{7}$$

Where

- I_{LPP} is the inductor peak-to-peak current
- L is the inductance of inductor
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Therefore, the peak switching current of inductor, I_{LPEAK}, is calculated as in equation 8.

$$C \quad C \quad \frac{C}{6} \tag{8}$$

Set the current limit of the SCT1270F higher than the peak current I_{LPEAK} and select the inductor with the saturation current higher than the current limit.

ol 'puk j vyz'KJ'y zpz hujl '/KJ Y0huk' ol 'j vy'svzz'zpnupmjhu s'hmmhj ' ol 'l mpjpb uj 'vmhww~l y'jvu l yzpvu5Jvy' loss is related to the core material and different inductors have different core loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss. Usually, a data sheet of an inductor does not provide the ESR and core loss information. If needed, consult the inductor vendor for detailed pumwyt h pvu5 ol y' pz' h' yhkl vmhht vun' ol 'puk j vyz' inductance, DCR and ESR resistance, and its footprint. Shielded inductors typically have higher DCR than unshielded inductors. Table 4 lists recommended inductors for the SCT1270F. Verify whether the recommended inductor can support the user's target application with the previous

Loop Stability

An external loop compensation network comprises resister R5, ceramic capacitors C5 and C6 connected to the COMP pin to optimize the loop response of the converter. The power stage small signal loop response of constant off time with peak current control can be modeled by equation 11.

$$A \quad \frac{L \quad 5}{6 \quad L} \quad \frac{5 \;\_\_\_\_ \; 5 \;\_\_\_\_}{5 \;\_\_\_}$$ (11)

where

- D is the switching duty cycle.
- R_{load} is the output load resistance.
- R_{SENSE} is the equivalent internal current sense resistor, which is 0.14 5

$$\frac{5}{6 \quad L}$$ (12)

where

- C_O is the output capacitance

$$\frac{5}{6 \quad L}$$ (13)

where

- ESR is the equivalent series resistance of the output capacitor.

$$\frac{L \quad 5}{6}$$ (14)

The COMP pin is the output of the internal trans-conductance amplifier. Equation 15 shows the small signal transfer function of compensation network.

$$A \quad \frac{A \quad L \quad P}{P} \quad \frac{5 \;\_\_\_\_}{5 \;\_\_\_\_ \; 5 \;\_\_\_\_}$$ (15)

where

- G_{EA} pz' ol 'ht wspb yz' yhuz-conductance
- R_{EA} pz' ol 'ht wspb yz' v w 'yl zpz hujl
- V_{REF} is the reference voltage at the FB pin
- V_{OUT} is the output voltage
- $_{COMP1}$ 3 $_{COMP2}$ are the poles' frequency of the compensation network.
- R

$$\frac{L}{L} \tag{18}$$

If the calculated value of C6 is less than 10pF, it can be left open. Designing the loop for greater than 45°of phase margin and greater than 10-dB gain margin eliminates output voltage ringing during the line and load transient.

Application Waveforms

Vin=3.6V, Vout=9V, unless otherwise noted

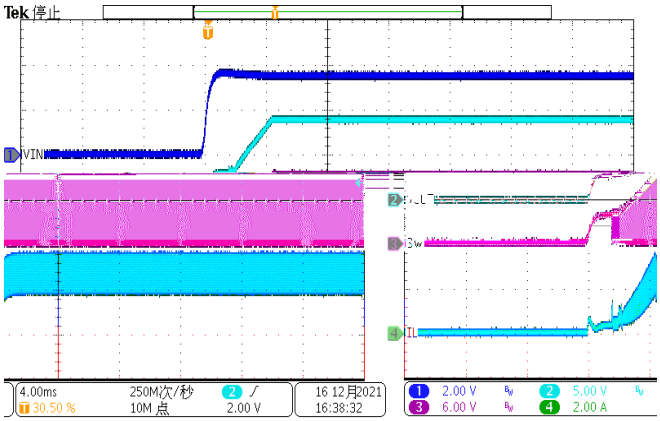

Figure 9. Power up

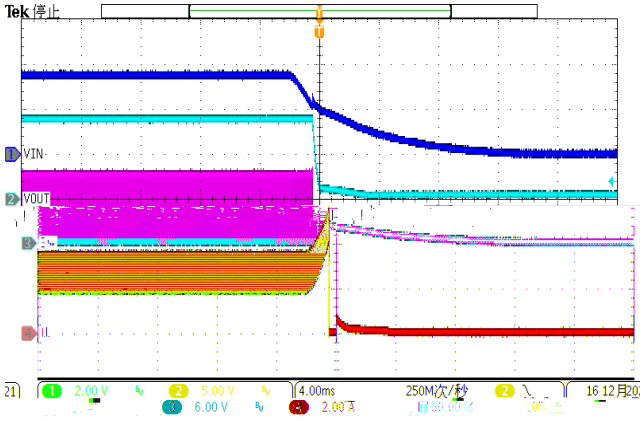

Figure 10. Power down

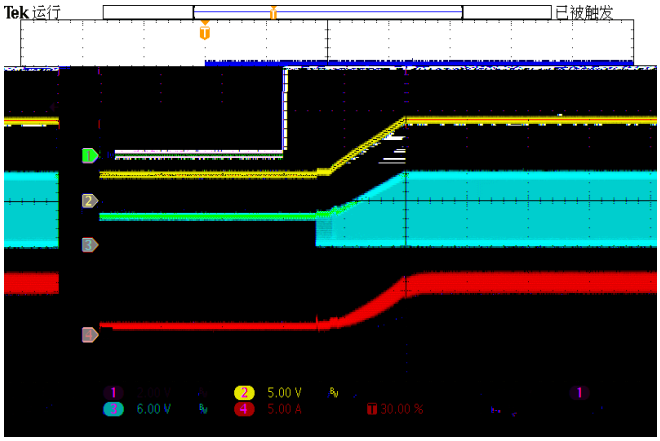

Figure 11. EN Power up (Iload=2A)

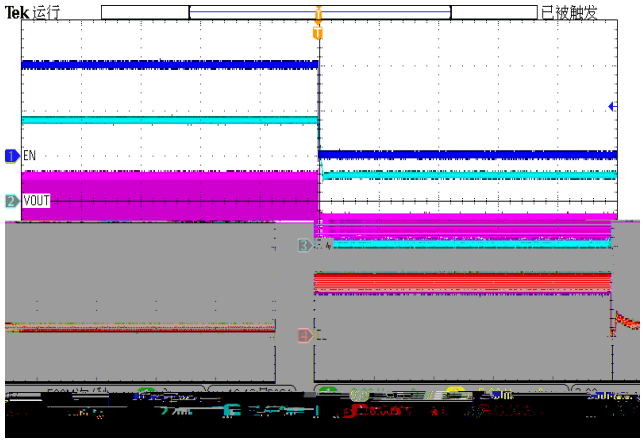

Figure 12. EN Power down(2A)

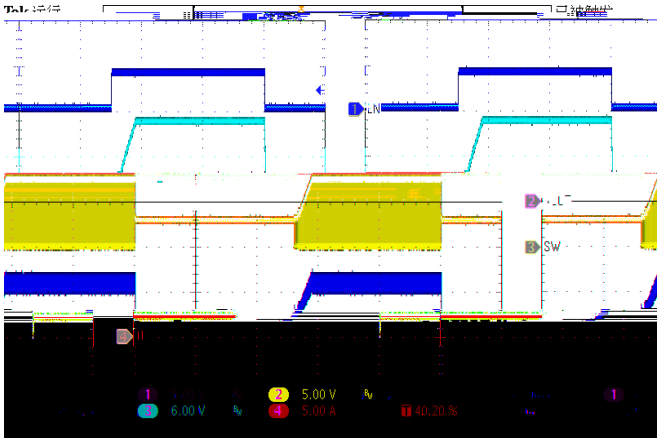

Figure 13. EN toggle (Iload=2A)

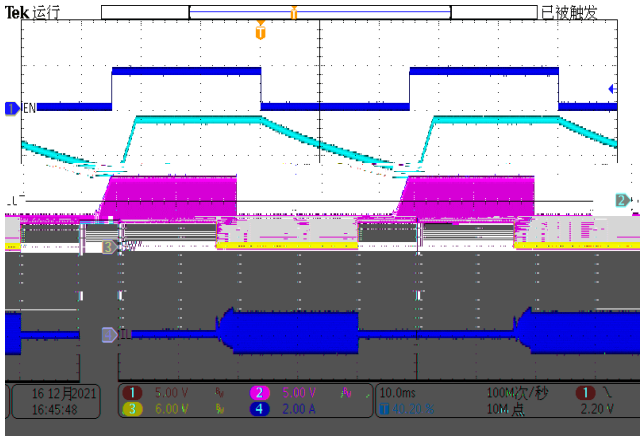

Figure 14. EN toggle (Iload=10mA)

Layout Guideline

The regulator could suffer from instability and noise problems without careful layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be close to the VIN pin and ground pad to reduce the input supply ripple.

The most critical current path for all boost converters is from the switching FET, through the rectifier FET, then the output capacitors, and back to ground of the switching FET. This high current path contains nanosecond rise time and fall time, and should be kept as short as possible. Therefore, the output capacitor needs not only to be close to the VOUT pin, but also to the GND pin to reduce the overshoot at the SW pin and VOUT pin. The placement and ground trace for output capacitor is critical for the performance of SW ringing voltage. Place the 0.1uF output capacitor as close to VOUT pins and power ground pad as possible to reduce high frequency ringing voltage on SW pin.

The layout should also be done with well consideration of the thermal. The SW, VOUT and GND pad under the chip should always be soldered well to the board for thermal, mechanical strength and reliability. Improper soldering will cause SW higher ringing and overshoot besides downgrading thermal performance.

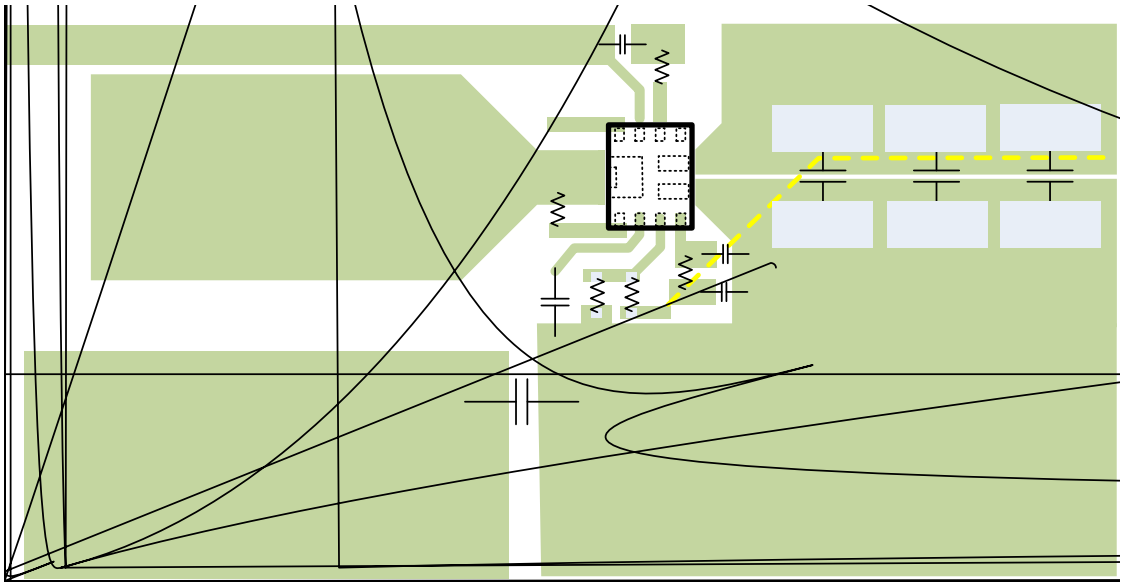

Figure 21. PCB Layout Example Top Layer

Thermal Considerations

The maximum IC junction temperature should be restricted to 150°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation 19.

$$\frac{5}{L} \tag{19}$$

where

- T_A is the maximum ambient temperature for the application.
- $R_{\theta H}$ is the junction-to-ambient thermal resistance given in the Thermal Information table.

SCT1270F QFN package includes a thermal pad that improves the thermal capabilities of the package. The real junction-to-ambient thermal resistance $R_{\theta H}$ of the package greatly depends on the PCB type, layout, thermal pad connection and environmental factor. Using thick PCB copper and soldering the thermal pad to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

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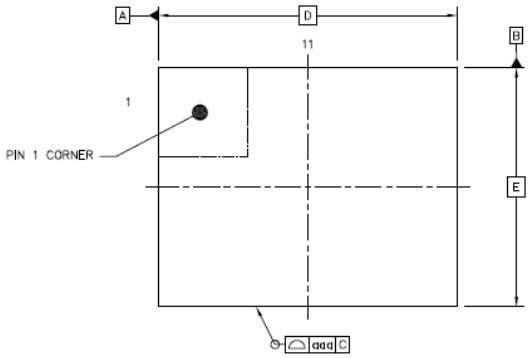
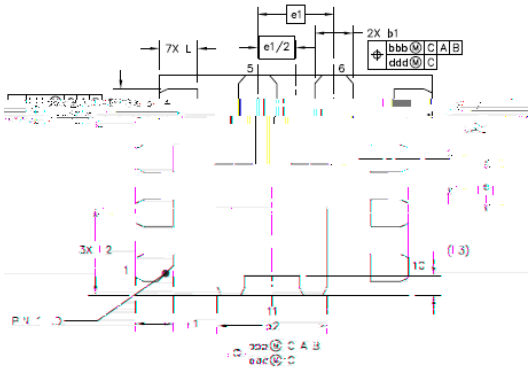
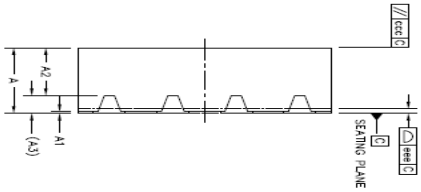


TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	---	0.55	---
A3		0.203 REF	
b	0.20	0.25	0.30
b1	0.30	0.35	0.40
b2	0.95	1	1.05
D		2.5 BSC	
E		2 BSC	
e		0.5 BSC	
e1		0.7 BSC	
L	0.3	0.35	0.4
L1	0.25	0.35	0.45
L2	0.75	0.8	0.85
L3		0.18 REF	
aaa		0.1	
ccc		0.1	
eee		0.05	
bbb		0.1	
ddd		0.05	

L H F DAF G E LAGF