3.8V-32V Vin, 500KHz, 2A Synchronous Step-down DCDC Converter with EMI Reduction

FEATURES

- EMI Reduction with Switching Node Ringing-free
- 3.8V-32V

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Release to market

Revision 1.1: Add low side FET leakage in EC table

Revision 1.2: Format adjustment

Revision 1.3: Update Device Order Information

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GND	7	Power ground. Must be soldered directly to ground plane.
SW	8	Switching node of the buck converter.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.8	32	V
T_J	Operating junction temperature	-40	125	°C

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ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		3.8		32	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising		3.5 420	3.7	V mV
I_{SD}						

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TYPICAL CHARACTERISTICS

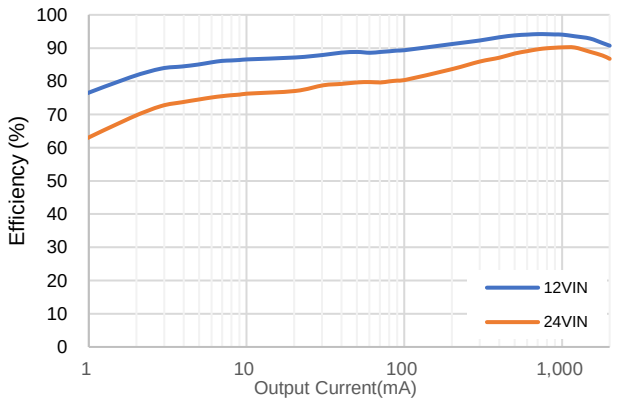

Figure 1. Efficiency, Vout=5V

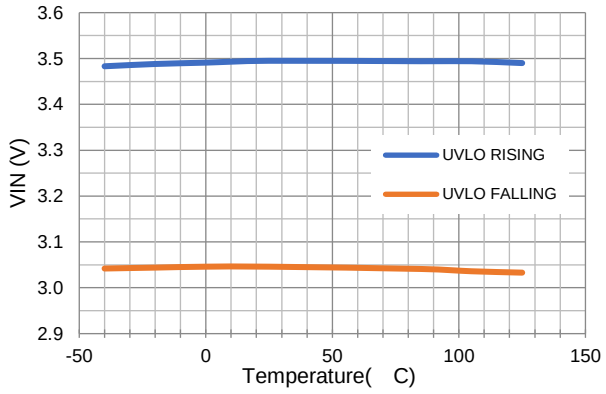

Figure 2. VIN UVLO vs Temperature

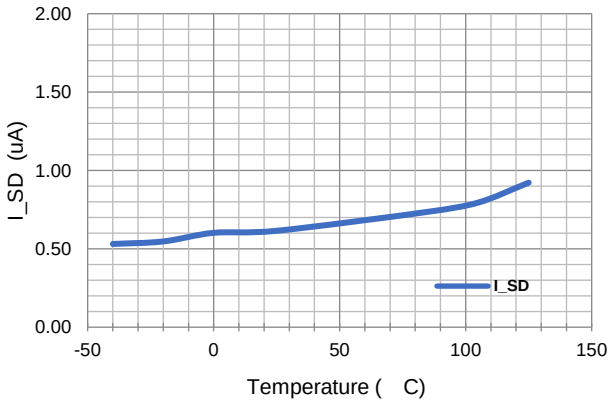

Figure 3. Shut down Current vs Temperature

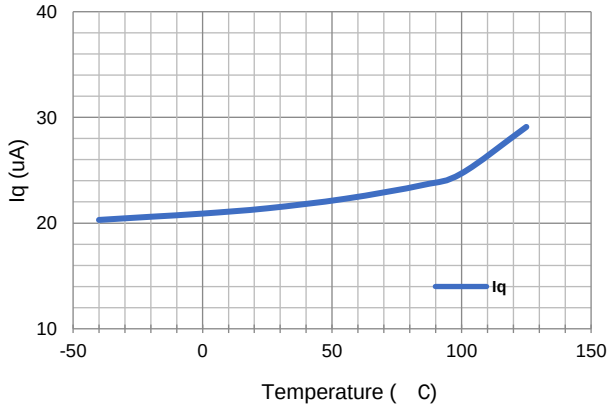

Figure 4. Quiescent Current vs Temperature

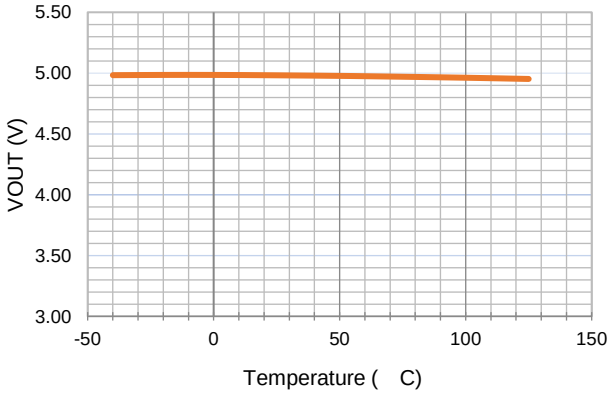

Figure 5. Output Voltage vs Temperature

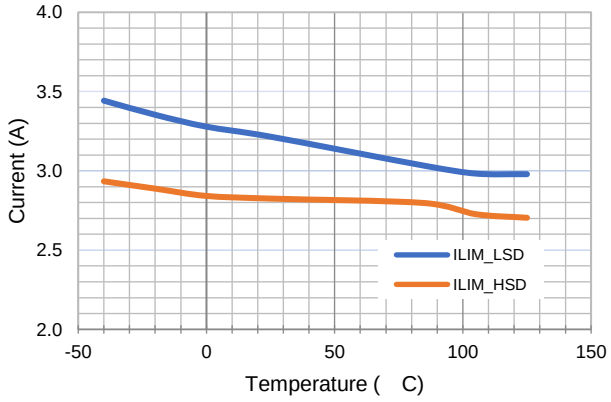

Figure 6. Peak Current Limit vs Temperature

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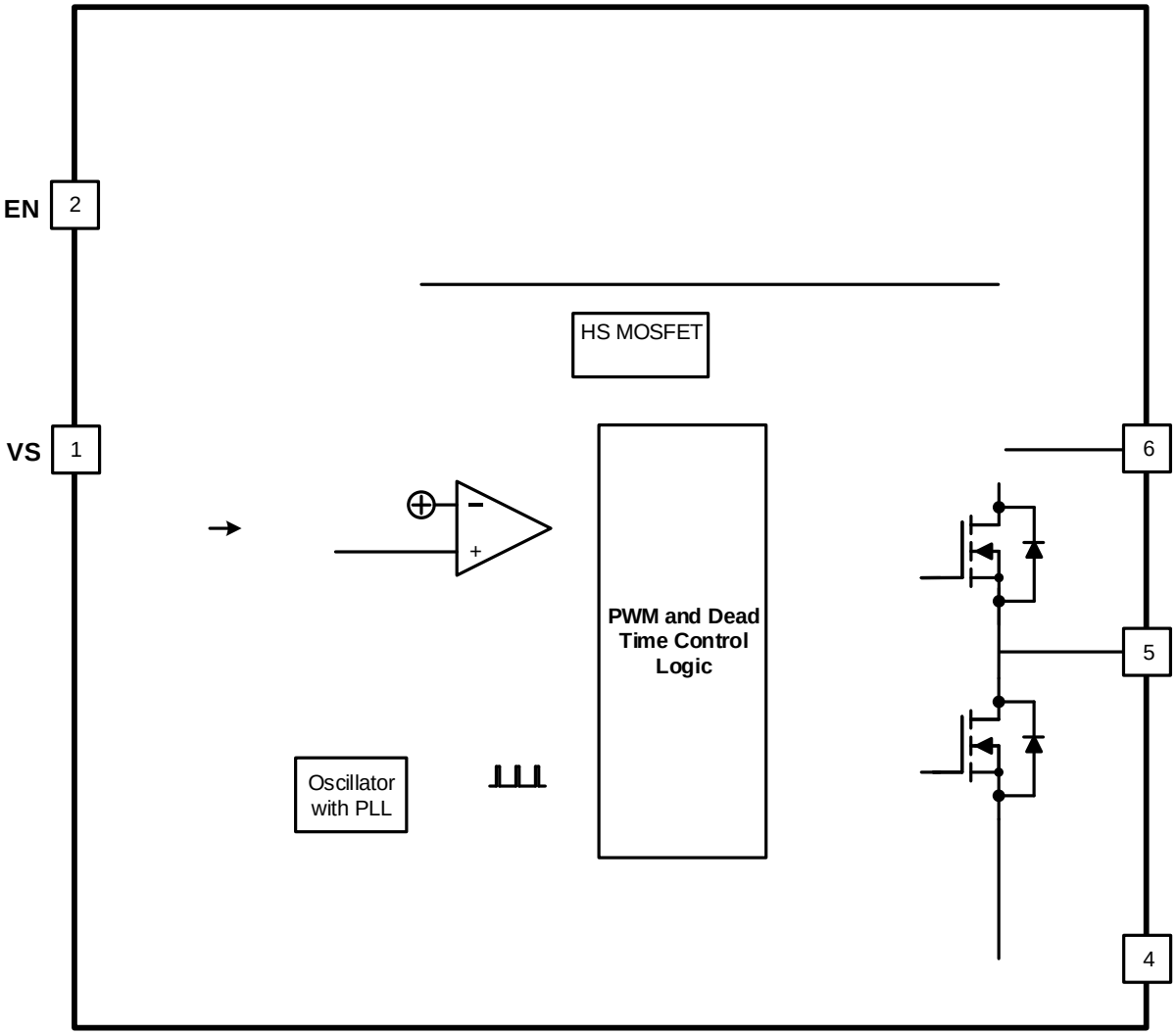
FUNCTIONAL BLOCK DIAGRAM



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OPERATION

Overview

The SCT9325 devices are 3.8V-32V input, 2A output, EMI friendly, fully integrated synchronous buck converter. The device employs fixed frequency peak current mode control. An internal clock with 500KHz frequency initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly and the converter charges output cap. When sensed voltage on high-side MOSFET peak current rising above the voltage of internal COMP (see functional block diagram), the device turns off high-side MOSFET Q1 and turns on low-side MOSFET Q2. The inductor current decreases when MOSFET Q2 is ON. In the next rising edge of clock cycle, the low-side MOSFET Q2 turns off. This repeats on cycle-by-cycle based.

The peak current mode control with the internal loop compensation network and the built-in 4ms soft-start simplify the SCT9325 footprints and minimize the off-chip component counts. The SCT9325 integrate the output voltage feedback resistor divider network to further simplify the off-chip components design. The SCT9325 has 5V output.

The error amplifier serves the COMP node by comparing the voltage on the VS pin with an internal reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The quiescent current of SCT9325 is 20uA typical under no-load condition and no switching. When disabling the device, the supply shut down current is only 1 The SCT9325 work at Pulse Skipping Mode (PSM) to further increase the power efficiency in light load condition. Hence the power efficiency can be achieved up to 88% at 5mA load condition.

The STC9325 implement the Frequency Spread Spectrum (FSS) modulation spreading of ±6% centered 500KHz switching frequency. FSS improves EMI performance by not allowing emitted energy to stay in any one receiver band for a significant length of time. The converter has optimized gate driver scheme to achieve switching node voltage ringing-free without sacrificing the MOSFET switching time to further damping high frequency radiation EMI noise.

The hiccup mode minimizes power dissipation during prolonged output over current or short conditions. The hiccup wait time is 512 cycles and the hiccup restart time is 8192 cycles. The SCT9325 device also features full protections including cycle-by-cycle high-side MOSFET peak current limit, over-voltage protection, and over-temperature protection.

VIN Power

The SCT9325 are designed to operate from an input voltage supply range between 3.8V to 32V, at least 0.1uF decoupling ceramic cap is recommended to bypass the supply noise. If the input supply locates more than a few inches from the converter, an additional electrolytic or tantalum bulk capacitor or with recommended 22uF may be required in addition to the local ceramic bypass capacitors.

Under Voltage Lockout UVLO

The SCT9325 feature Under Voltage Lock Out(UVLO) functions. The default startup threshold is typical 3.5V with VIN rising and shutdown threshold is 3.1V with VIN falling. The more accurate UVLO threshold can be programmed through the precision enable threshold of EN pin.

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Enable and Start up

When applying a voltage higher than the EN high threshold (typical 1.18V rising), the SCT9325 enable all functions and the devices start soft-start phase. The SCT9325 have the built-in 4ms soft-start time to prevent the output overshoot and inrush current. When EN pin is pulled low, the internal SS net will be discharged to ground. Buck operation is disabled when EN voltage falls below its lower threshold (typically 1.1V falling).

An internal 1.5uA pull up current source connected from internal LDO power rail to EN pin guarantees that floating EN pin automatically enables the device. For the application requiring higher VIN UVLO voltage than the default setup, there is a 4uA hysteresis pull up current source on EN pin which configures the VIN UVLO voltage with an off-chip resistor divider R3 and R4, shown in Figure 7. The resistor divider R3 and R4 are calculated by equation (1) and (2).

EN pin is a high voltage pin, and can be directly connected to VIN to automatically start up the device with VIN rising to its internal UVLO threshold.

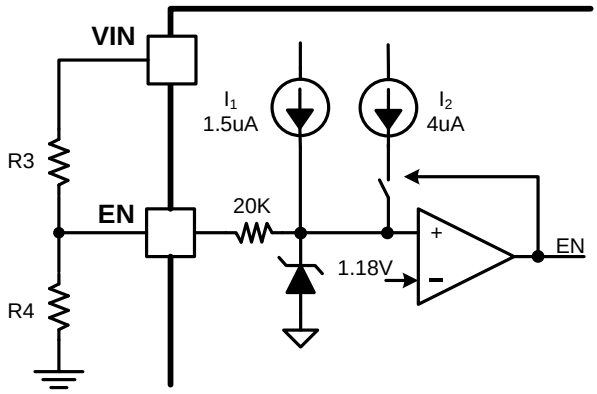

Figure 7. Adjustable VIN UVLO

(1)

(2)

Where,
Vstart: Vin rise threshold to enable the device
Vstop: Vin fall threshold to disable the device
I_1=1.5uA
I_2=4uA
V_{ENR}=1.18V
V_{EMF}=1.1V

EMI Reduction with Frequency Spread Spectrum and Switching Node Ringing-free(Patent)

In the some applications, the system EMI test must meet EMI standards EN55011 and EN55022. dTQ EMC /P AMCID 3 37>0

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band and therefore reduces conducted and radiated interference peak amplitude at a particular frequency. The SCT9325 feature 500KHz switching frequency with spreading frequency of +/-6% and modulation rate 1/512 of switching frequency. The FSS technique effectively decreases the EMI noise by spreading the switching frequency from fixed 500KHz. As a result, the harmonic wave amplitude is reduced and the harmonic wave band is wider.

In buck converter, the switching node ringing amplitude and cycles are critical especially related to the high frequency radiation EMI noise. The SCT9325 implement the multi-level gate driver speed technique to achieve the switching node ringing-free without scarifying the switching node rise/fall slew rate and power efficiency of the converter. The switching node ringing amplitude and cycles are damped by the built-in MOSFETs gate driving technique (SCT Proprietary Design). The switching node zoomed in wave form is shown in Figure 8.

Figure 8. Switching Node Waveform

Peak Current Limit and Hiccup Mode

The SCT9325 have cycle-by-cycle peak current limit with sensing the internal high side MOSFET Q1 current during over current condition. While the Q1 turns on, its conduction current is monitored by the internal sensing circuitry. Once the high-side MOSFET Q1 current exceeds the limit, it turns off immediately. If the Q1 over current time exceeds 512 switching cycles (hiccup waiting time), the buck converter enters hiccup mode and shuts down. After 8192 cycles off, the buck converter restarts to power up. The hiccup modes reduce the power dissipation in over current condition.

Over Voltage Protection and Minimum On-time

The SCT9325 feature the output over-voltage protection (OVP). If the output pin voltage exceeds 110% of reference output voltage, the converter stops switching immediately. When the output feedback pin voltage drops below 105% of set output voltage, the converter resumes to switching. The OVP function prevents the connected output circuitry damaged from un-predictive overvoltage. Featured feedback overvoltage protection also prevents dynamic voltage spike to damage the circuitry at load during fast loading transient.

The high-side MOSFET Q1 has minimum on-time 80ns typical limitation. While the device operates at minimum on-time, further increasing VIN results in pushing output voltage beyond regulation point. With output feedback over voltage protection, the converter skips pulse by turning off high-side MOSFET Q1 and prevents output running away higher to damage the load.

Pulse Skipping Modulation PSM Mode

In heavy load condition, the SCT9325 force the device operating at forced Pulse Width Modulation (PWM) mode. When the load current decreasing, the internal COMP net voltage decreases as the inductor current down. With the load current further decreasing, the COMP net voltage decreases and be clamped at a voltage corresponding to the 450mA peak inductor current. When the load current approaches zero, the SCT9325 enter Pulse Skipping Modulation (PSM) mode to increase the converter power efficiency at light load condition. When the inductor current decreases to zero, zero-cross detection circuitry on high-side MOSFET Q1 forces the Q1 off till the beginning of the next switching cycle. The buck converter does not sink current from the load when the output load is light and converter works in PSM mode.

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Bootstrap Voltage Regulator

An external bootstrap capacitor between BST and SW pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

The floating supply (BST to SW) UVLO threshold is 2.7V rising and hysteresis of 350mV. When the converter operates with high duty cycle or prolongs in sleep mode for certain long time, the required time interval to recharging bootstrap capacitor is too long to keep the voltage at bootstrap capacitor sufficient. When the voltage across bootstrap capacitor drops below 2.35V, BST UVLO occurs. The SCT9325 intervene to turn on low side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee operation over a wide duty range.

Low Drop-Out LDO Regulation

To support the application of small voltage-difference between Vout and Vin, the Low Drop Out (LDO) Operation is implemented by the SCT9325. The Low Drop Out Operation is triggered automatic when the off time of the high-side power MOSFET exceeds the minimum off time limitation.

In low drop out operation, high-side MOSFET remains ON as long as the BST pin to SW pin voltage is higher than BST UVLO threshold. When the voltage from BST to SW drops below 2.35V, the high-side MOSFET turns off and low-side MOSFET turns on to recharge bootstrap capacitor periodically in the following several switching cycles. Only 100ns of low side MOSFET turning on in each refresh cycle minimizes the output voltage ripple. Low-side MOSFET may turn on for several times till bootstrap voltage is charged to higher than 2.7V for high-side

MOSFET working normally. Then high-side MOSFET turns on and remains on until bootstrap voltage drops to trigger bootstrap UVLO again. Thus, the effective duty cycle of the switching regulator during Low Drop-out LDO operation can be very high even approaching 100% as shown in Figure 9.

During ultra-low voltage difference of input and output voltages, i.e. the input voltage ramping down to power down, the output can track input closely thanks to LDO operation mode.

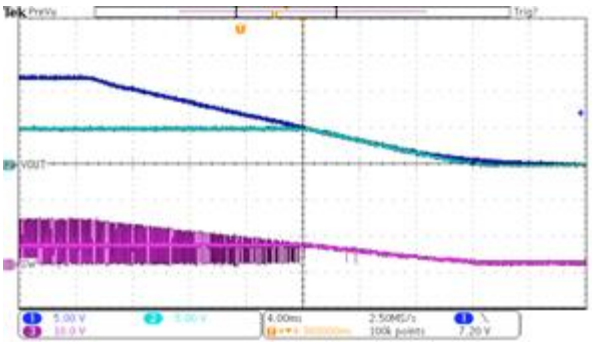

Figure 9. SCT9325 LDO Mode Waveform

Thermal Shutdown

Once the junction temperature in the SCT9325 exceeds 160C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 125C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

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APPLICATION INFORMATION

Typical Application

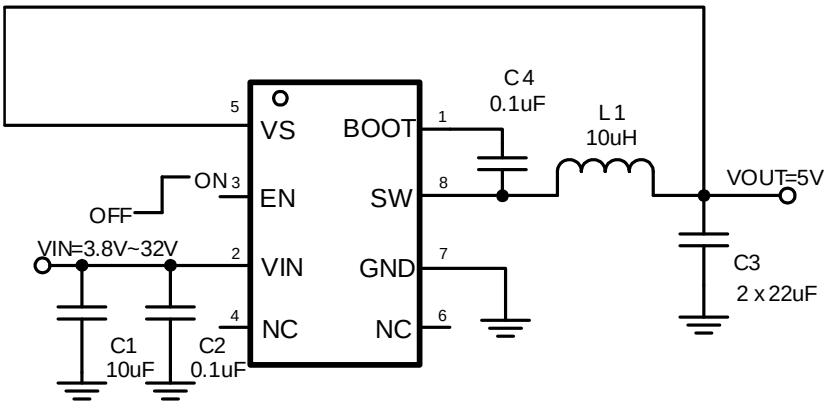

Figure 10. 12V Input, 5V/2A Output

Design Parameters

Design Parameters	Example Value
Input Voltage	12V
Output Voltage	5V
Output Current	2A
Output voltage ripple (peak to peak)	±0.3V
Switching Frequency	500KHz

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Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A ceramic capacitor 10 for the decoupling capacitor and a 0.1 to be placed as close as possible to the VIN pin of the SCT9325.

Use Equation (3) to calculate the input voltage ripple:

(3)

Where:

- C_{IN} is the input capacitor value
- f_{sw} is the converter switching frequency
- I_{OUT} is the maximum load current

Due to the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the VIN pin. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, a 35V/10uF input ceramic capacitor is recommended for most of applications. Choose the right capacitor value carefully with considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Inductor Selection

The performance of avior, loop stability, and buck converter efficiency. The inductor value, DC resistance (DCR), and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DCR, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the maximum input voltage, minimum output voltage, maxim load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a buck converter, calculate the inductor minimum value as shown in equation (4).

(4)

Where:

- K_{IND} is the coefficient of inductor ripple current relative to the maximum output current.

Therefore, the peak switching current of inductor, I_{LPEAK}, is calculated as in equation (5).

(5)

Set the current limit of the SCT9325 higher than the peak current I_{LPEAK} and select the inductor with the saturation current higher than the current limit. The the core loss significantly affect the efficiency of power conversion. Core loss is related to the core material and different inductors have different core

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loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss.

Table 1 lists recommended inductors for the SCT9325. Verify whether the recommended inductor can support the user's target application with the previous calculations and bench evaluation. In this application, the WE's inductor 744314101 is used on SCT9325 evaluation board.

Table 1. Recommended Inductors

Part Number	L (uH)	DCR Max	Saturation Current/Heat Rating Current (A)	Size Max (LxWxH mm)	Vendor
744314101	10	33	3.5	7x7x5	Wurth Electronik

Output Capacitor Selection

For buck converter, the output capacitor value determines the regulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

For small output voltage ripple, choose a low-ESR output capacitor like a ceramic capacitor, for example, X5R and X7R family. Typically, 1 3x 22
can be used to improve the load transient response. Due to de-rating under DC bias, the bias can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance.

From the required output voltage ripple, use the equation (6) to calculate the minimum required effective capacitance, C_{OUT}.

(6)

Where

- $V_{OUTRipple}$ is output voltage ripple caused by charging and discharging of the output capacitor.
- I_{LPP} is the inductor peak to peak ripple current, equal to $k_{IND} * I_{OUT}$.
- $_{SW}$ is the converter switching frequency.

The allowed maximum ESR of the output capacitor is calculated by the equation (7).

(7)

The output capacitor affects $_{C}$. Considering the loop stability and effect of the internal loop compensation parameters, choose the crossover frequency less than 55 kHz (—) without considering the feed-forward capacitor. A simple estimation for the crossover frequency without feed forward capacitor is shown in equation (8), assuming C_{OUT} has small ESR.

(8)

Where

- G_M is the transfer conductance of the error amplifier (300uS).

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- G_{MP} is the gain from internal COMP to inductor current, which is 5A/V.
- f_C is the cross over frequency.

Additional capacitance de-rating for aging, temperature and DC bias should be factored in which increases this minimum value. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. The capacitor data sheets specify the RMS (Root Mean Square) value of the maximum ripple current. Equation (9) can be used to calculate the RMS ripple current the output capacitor needs to support.

(9)

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Application Waveforms

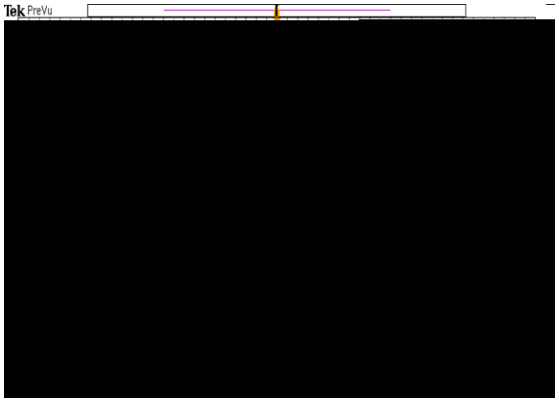

Figure 11. SW node waveform and Output Ripple, Iout=2A

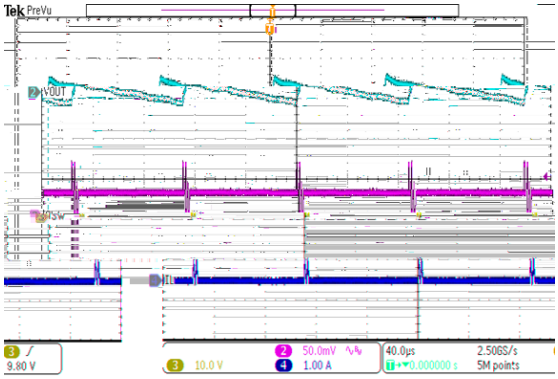

Figure 12. SW node Waveform and Output Ripple, Iout=10mA

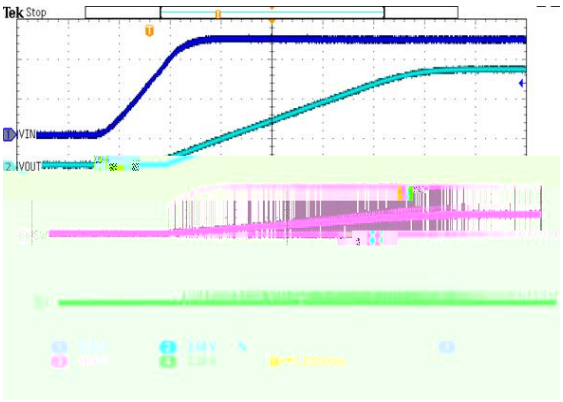

Figure 13. Power Up, Iout=10mA

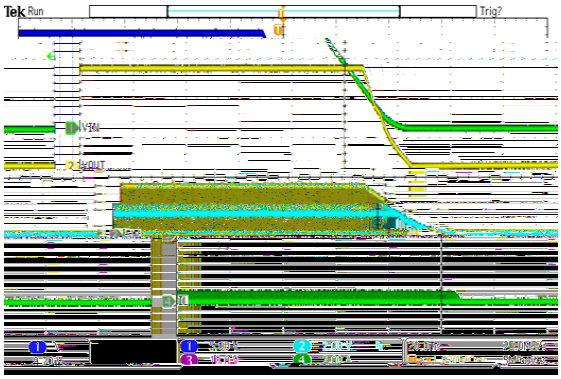

Figure 14. Power Down, Iout=10mA

Figure 15. Load Transient
(Vout=5V, Iout=0.2A to 1.8A, SR=250mA/us)

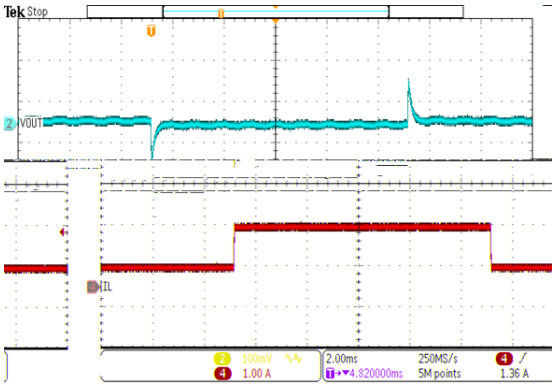

Figure 16. Load Transient
(Vout=5V, Iout=0.5A to 1.5A, SR=250mA/us)

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Layout Guideline

The regulator could suffer from instability and noise problems without carefully layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be very close to the VIN pin and GND pin to reduce the input supply ripple. Place the capacitor as close to VIN pin as possible to reduce high frequency ringing voltage on SW pin as well. Figure 17 is the recommended PCB layout of the SCT9325.

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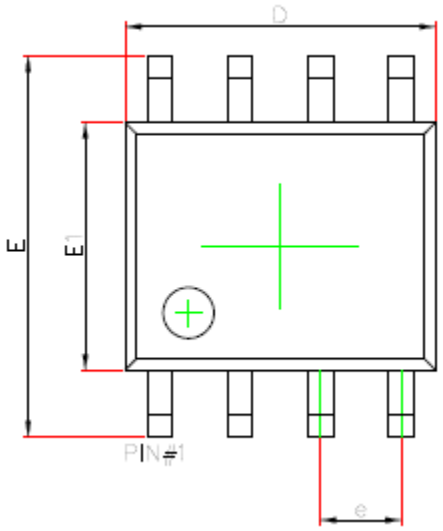
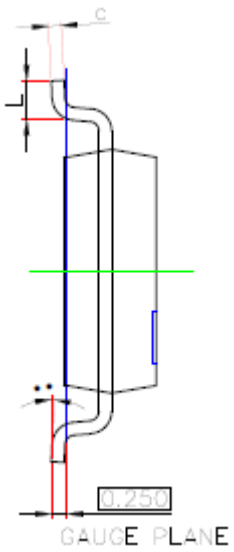
clTOT0.87 619.06 Tm0 g0OT0.86bm

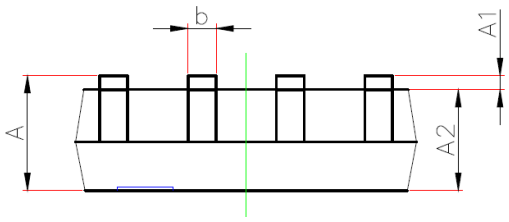
PACKAGE INFORMATION



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	1.35		1.75
A1	0.1		0.25
A2	1.35		1.55
D	4.8		5
E	5.8		6.2
E1	3.8		4.0
b	0.33		0.51
c	0.17		0.25
e	1.27(BSC)		
L	0.40		1.27
	0		8

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

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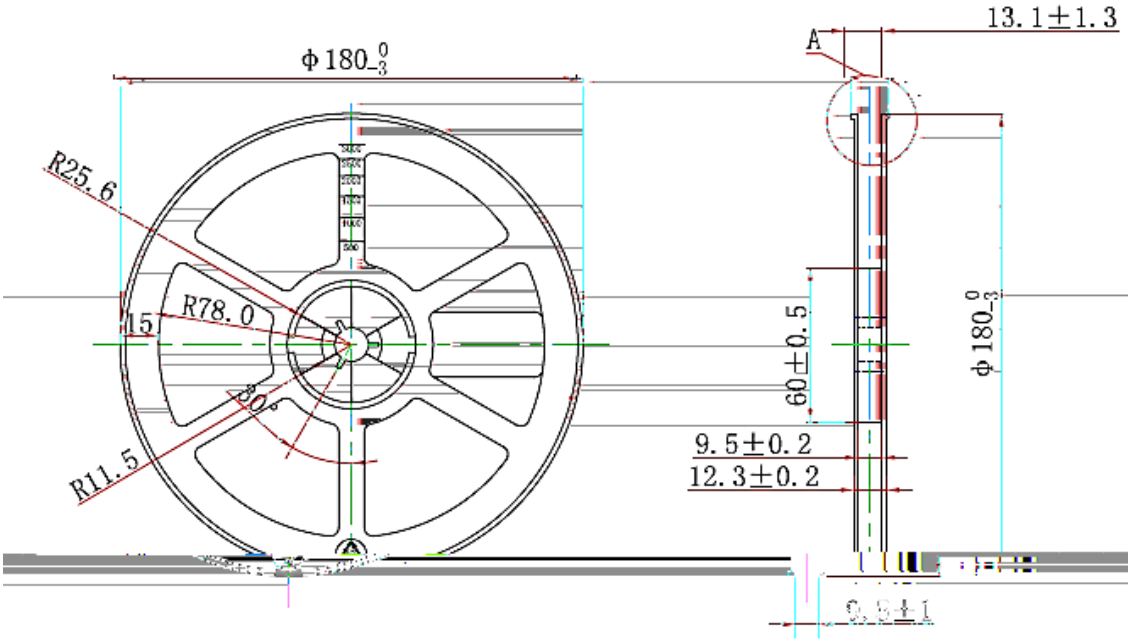
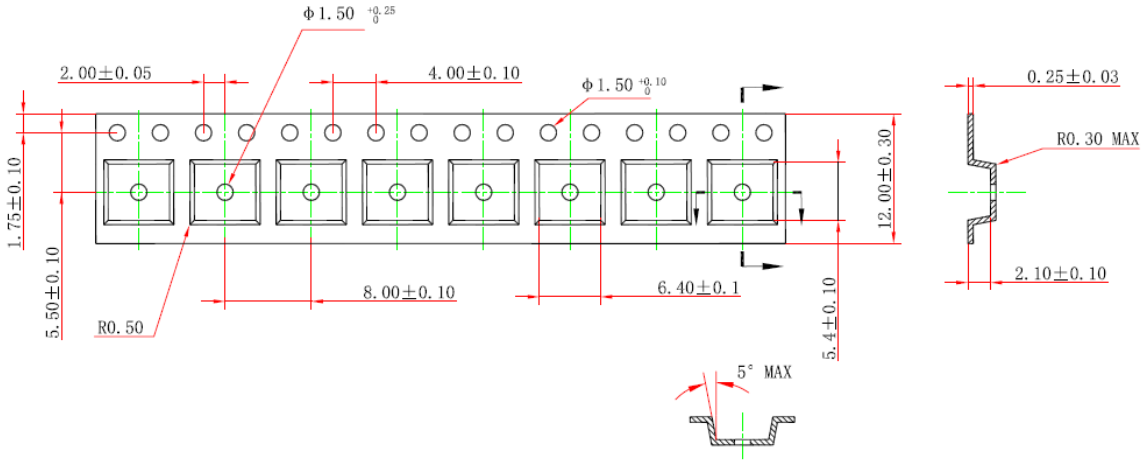
TAPE AND REEL INFORMATION





Feeding Direction

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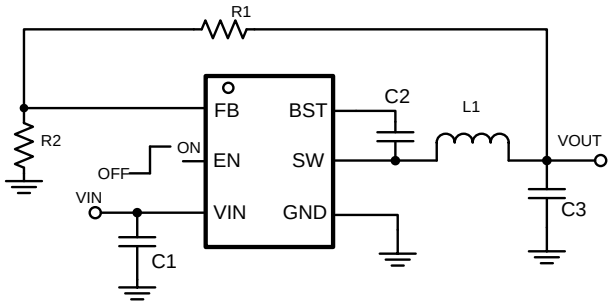
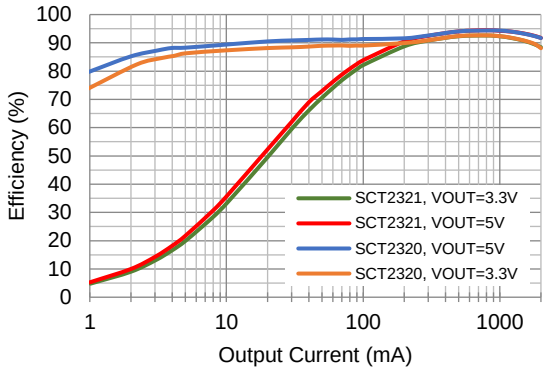
TYPICAL APPLICATION

24V Input, 5V Output, 500kHz Synchronous Buck Converter



Efficiency, VIN=12V



RELATED PARTS

PART NUMBERS	DESCRIPTION	COMMENTS
SCT2320 **SCT2330**	3.8V-32V Vin, 2A/3A, 500kHz Synchronous Buck Converter with EMI Reduction	• 20uA quiescent current • 500kHz switching frequency with ±6% frequency spread spectrum. • EMI reduction with switching node ringing-free.
SCT2321 **SCT2331**	3.8V-32V Vin, 2A/3A, 500kHz Synchronous Buck Converter with PWM Mode	• Forced PWM mode operation. • Fixed 500kHz Switching Frequency.

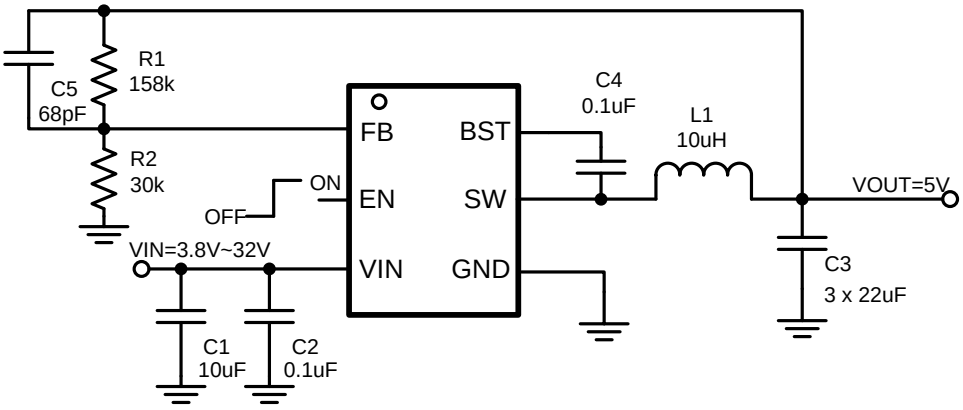


Figure 18. SCT2320 and SCT2321 Typical Application

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