5 to 60V Three-Phase Brushless DC Motor Pre-Driver

- Wide Operating Voltage: 5V to 60V
- Charge Pump Gate Drive Supply
- 100% Duty Operation with Trickle Charge Circuit
- 1A Maximum Peak Source Current
- 2A Maximum Peak Sink Current
- 3.3V and 5V Logic Compatible
- Low-Power Sleep Mode
- Adjustable Dead-Time
- Fault Indication Output
- Full Protection Features
  - Over Current Protection
  - Short Circuit Protection
  - Input Undervoltage Lockout
  - Gate Driver Undervoltage Lockout
  - Bootstrap Undervoltage Protection
  - Thermal Shutdown Protection
- Available in QFN-28L(4mm×4mm) Package.

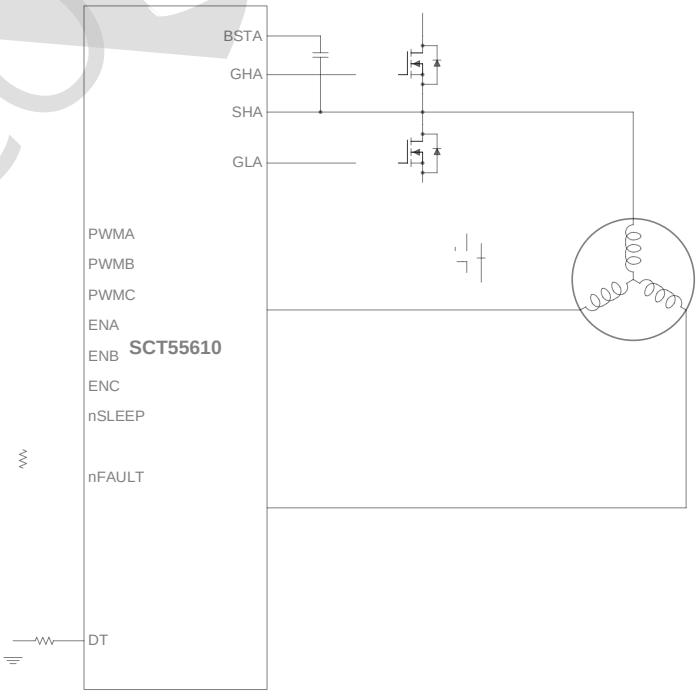
The SCT55610 is a highly integrated gate driver IC for three-phase Brushless DC(BLDC) motor control. It is capable of driving 3 high-side and 3 low-side N-channel MOSFETs with a wide input supply range from 5V to 60V.

The SCT55610 supports 100% duty operation with an internal trickle charge circuit to maintain high-side gate driver voltage. Low-power sleep mode is supported to achieve low stand-by current.

The SCT55610 provides full protection features, including over current protection, short circuit protection, input undervoltage lockout, gate driver undervoltage lockout, bootstrap undervoltage protection and thermal shutdown protection. Fault conditions are indicated through an open-drain output pin(nFAULT).

The device is available in 4mm×4mm QFN-28L package.

- Three-Phase Brushless DC Motor
- Fans and Pumps
- Drone
- Robot Vacuum



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NAME	PIN	PIN FUNCTION
VIN	1	Input supply voltage. Connect a bypass capacitor close to the pin.
CPA	2	Charge pump switching node. Connect a ceramic capacitor between CPA and CPB.

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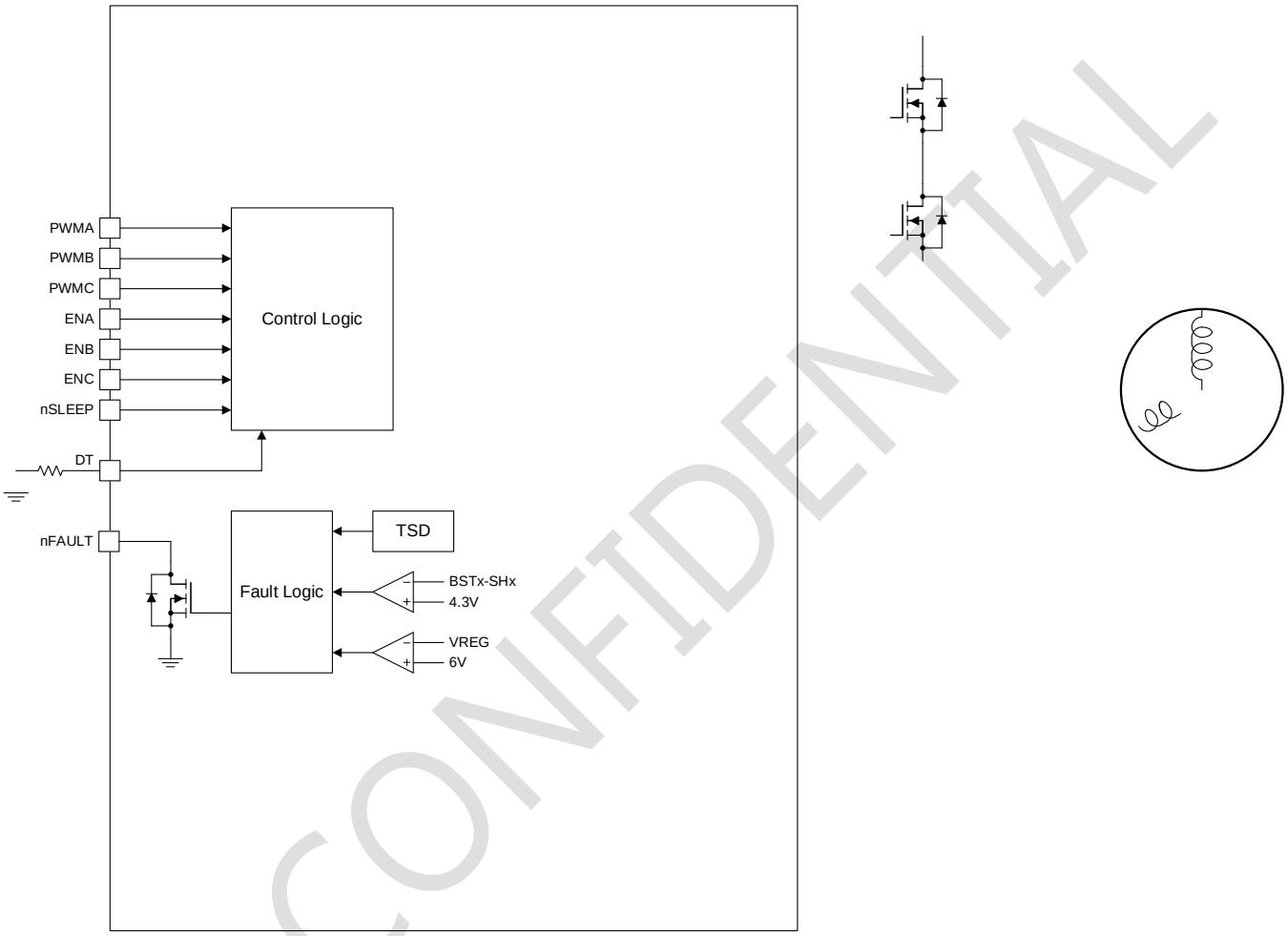

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Sleep Mode

The SCT55610 can enter a low-power sleep mode where most internal circuits are turned off to save power. All the gate drivers are disabled in sleep mode. The sleep mode is entered by pulling nSLEEP pin low, and exited by pulling nSLEEP pin high with a wakeup delay of around 250us. The nSLEEP pin has an internal pulldown so it must be pulled high for normal operation.

Over Current Protection

The SCT55610 protects the system from over-current failure by monitoring LSS pin voltage and timely shutting down when it is over 0.5V. The LSS pin is connected to the sources of the three low-side MOSFETs, and tied to ground through an external sense resistor, whose voltage drop equals the resistance multiplied by the total current of the three phases. For example, if a 50m sense resistor is used, the over current protection will be triggered once the total current exceeds 10A. When an over-current condition is detected for over 3us deglitch time, all the gate driver outputs are driven low immediately and nFAULT pin is pulled low. The SCT55610 will be latched in the fault state even after the over-current condition is gone, and only reset by toggling nSLEEP pin or power cycle.

Over current protection can be disabled by connecting LSS pin directly to ground or connecting SCREF pin to VREG

Short Circuit Protection

The SCT55610 protects the system from short-circuit failure by monitoring the drain-to-source voltage drop of the turned-on MOSFET through VIN, SHx and LSS pins. In a short-circuit case, the current running through the MOSFET immediately increases and so does the voltage across the MOSFET. When a voltage drop higher than the short-circuit threshold is detected for over 3us deglitch time, all the gate driver outputs are driven low immediately and nFAULT pin is pulled low. The short-circuit threshold is set by SCREF pin with an external voltage reference. The SCT55610 will be latched in the fault state even after the short-circuit condition is gone, and only reset by toggling nSLEEP pin or power cycle.

Short circuit protection can be disabled by .

Undervoltage Lockout Protection

The SCT55610 monitors VIN, VREG and bootstrap voltage and shuts down when any of them falls lower than its undervoltage lockout threshold. In these cases, the SCT55610 will pull all gate driver outputs low immediately, latched in the fault state and only reset by toggling nSLEEP pin or power cycle. See Electrical Characteristics table for detailed undervoltage lockout thresholds.

Thermal Shutdown

Once the junction temperature of SCT55610 exceeds 150ºC, the thermal sensing circuit shuts down the device. All the gate driver outputs are driven low immediately and nFAULT pin is pulled low. The SCT55610 will be latched in the fault state even after the over-temperature condition is gone, and only reset by toggling nSLEEP pin or power cycle. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

Fault Action and Response

The fault action and response of SCT55610 are listed in Table 2.

Table 2. Fault Action and Response

Fault	Condition	Report	Gate Driver	Recovery
VIN UVLO	V_{IN} < 4V	None	Pulled low	V_{IN} > 4.2V
VREG UVLO	V_{REG} < 6V	nFAULT	Pulled low	Latched
BST UVLO	BSTx - SWx < 4.3V and ENx = 1	nFAULT	Pulled low	Latched
Over-current	V_{LSS} > 0.5V	nFAULT	Pulled low	Latched
Short-circuit	V_{DS_ON} > V_{SCREF}	nFAULT	Pulled low	Latched
Thermal Shutdown	T_J > 150°C	nFAULT	Pulled low	Latched

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Driver Power Dissipation

Generally, the power dissipation in the SCT55610 depends on the driver-stage loss and V_{REG} regulation loss.

The power loss of a single gate driver can be estimated by Equation (2):

$$= \times \times \quad (2)$$

where

- Q_g is the total gate charge of the power device
- f_{SW} is the switching frequency
- V_{REG} is the gate drive voltage

If the gate resistor R_G applied between the driver output and gate of power device to slow down the switching transition, the power loss of a single gate driver can be estimated by Equation (3):

$$= \frac{1}{2} \times \times \times \times \frac{}{+} + \frac{}{+} \quad (3)$$

where

- R_{UP} is the gate driver pull-up resistance
- R_{DN} is the gate driver pull-down resistance
- R_G is the external resistance between the driver output and gate of power device

For a typical three-phase BLDC motor control, always only one of the three half-bridges are switching at f_{SW} during the whole rotation cycle. In this case, the total driver-stage power dissipation can be estimated by one half-bridge, namely a high-side gate driver and a low-side gate driver.

The gate drive voltage V_{REG} is generated from VIN through either a charge pump when VIN is low or a LDO when VIN is high. The power loss of V_{REG} regulation can be estimated referring to Table 3:

Table 3 V_{REG} Regulation Loss

Input Range	Mode	Power Loss Equation
VIN < 16V	Charge Pump	$= 2 \times \frac{}{} - 1 \times$
VIN > 16V	LDO	$= \frac{}{} - 1 \times$

Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation (4):

$$( ) = \frac{125 -}{\theta JA} \quad (4)$$

where

- T_A is the maximum ambient temperature for the application
- R_{JA} is the junction-to-ambient thermal resistance given in the Thermal Information table

The real junction-to-ambient thermal resistance R_{JA} of the package greatly depends on the PCB type, layout, and environmental factor. Soldering the ground pin to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

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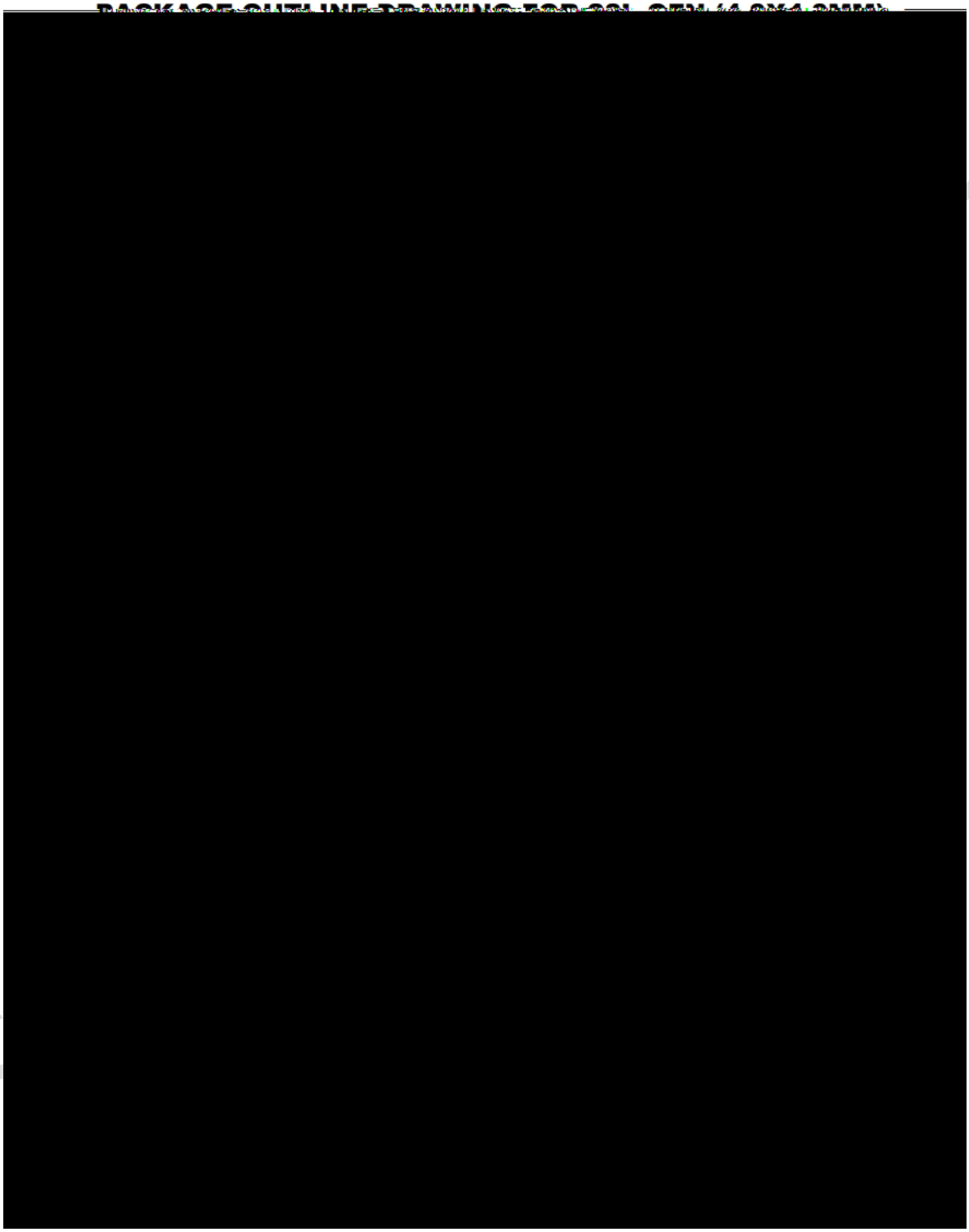

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